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MS-7C02 BOM List

Schematic Cfg	ERP NO.	Remark	BOM
CFG-7C02-01S-Arsenal Gaming	601-7C02-01S		A

★

 MICRO-STAR INT'L CO.,LTD.	
COVER SHEET	
Title Size Date	Document Number MS-7C02.. Tuesday, December 18, 2018
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AMD

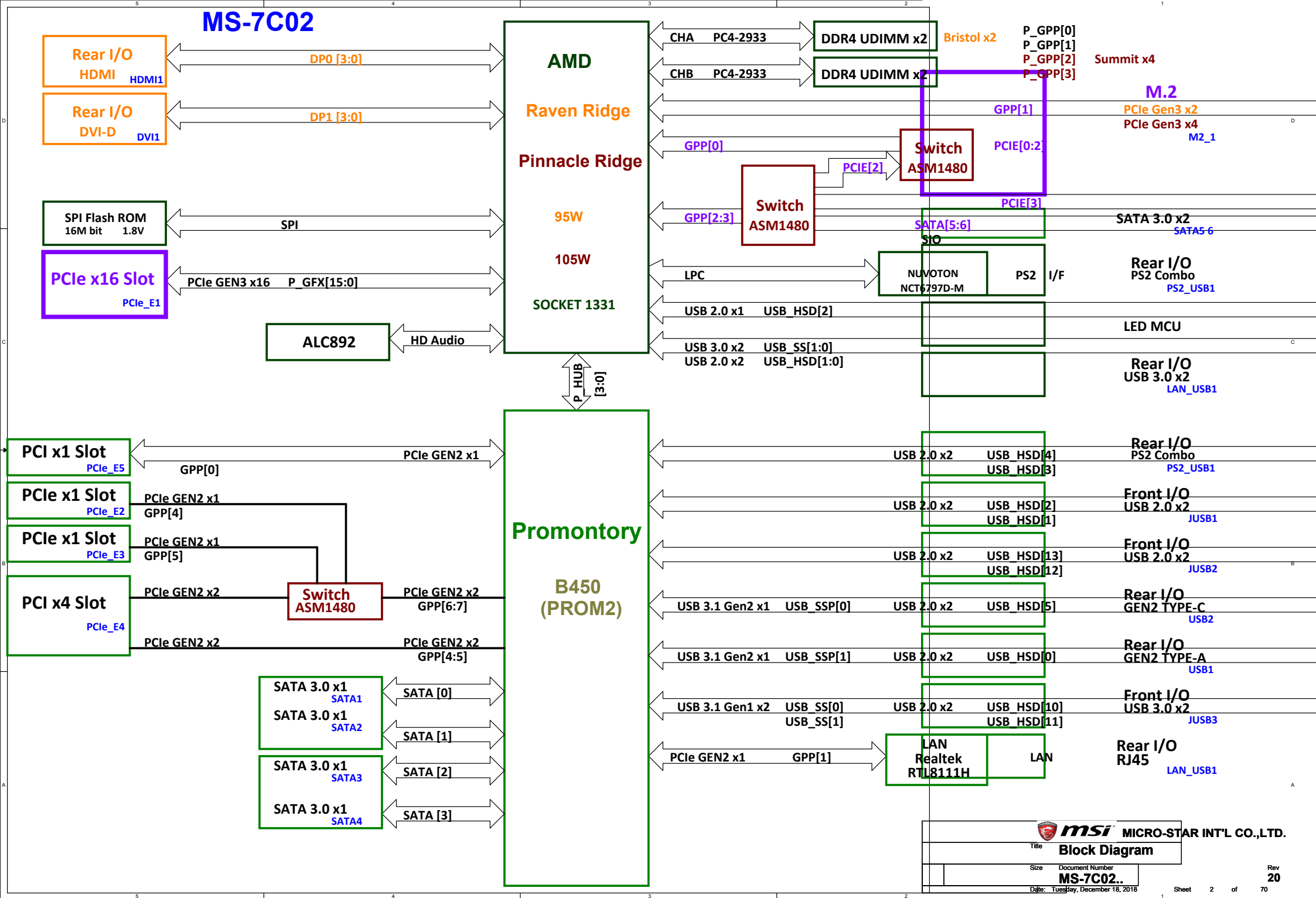
Raven Ridge

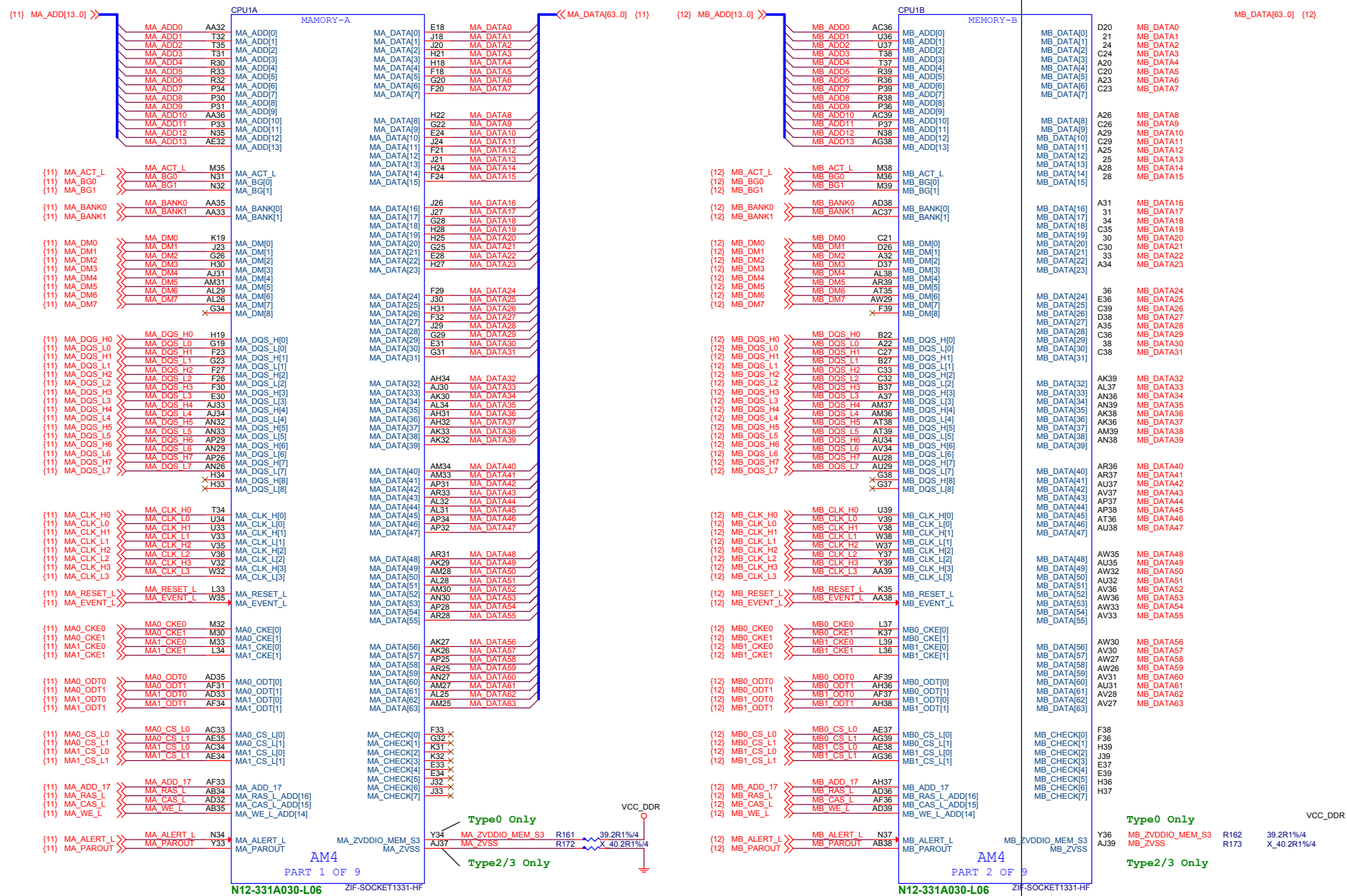
Pinnacle Ridge

95W

105W

SOCKET 1331





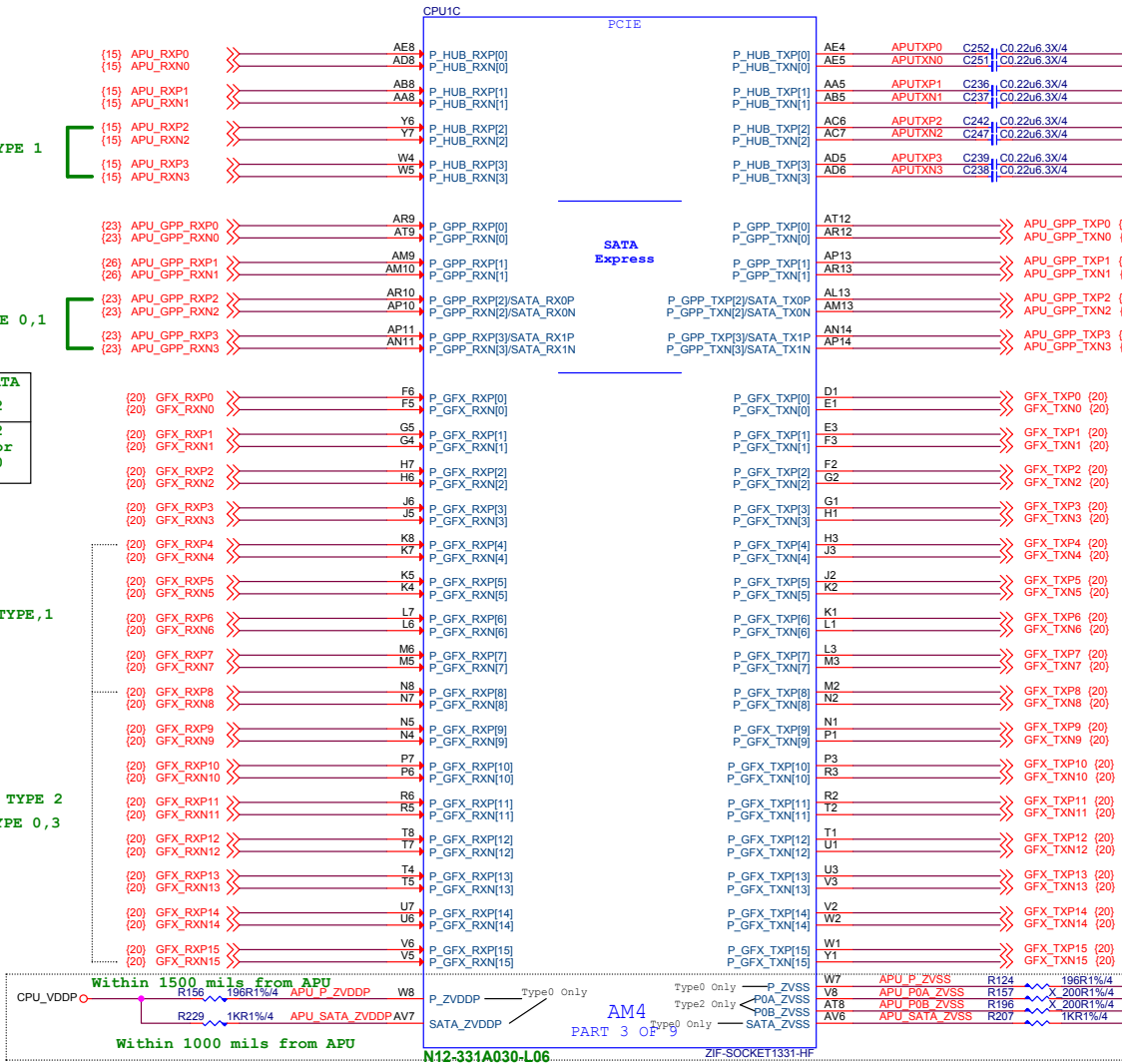
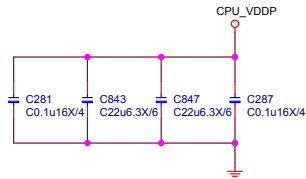
Not supported HUB on TYPE 1

Not supported PCIE on TYPE 0,1

TYPE 0	PCIE	SATA
	2	2
TYPE 2/3	2 or 4	2 or 0

Not supported GFX 4~15 on TYPE,1

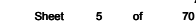
Only supported on TYPE 2
Not supported GFX 8~15 on TYPE 0,3



SATA5,SATA6
Not supported PCIE on TYPE 0,1

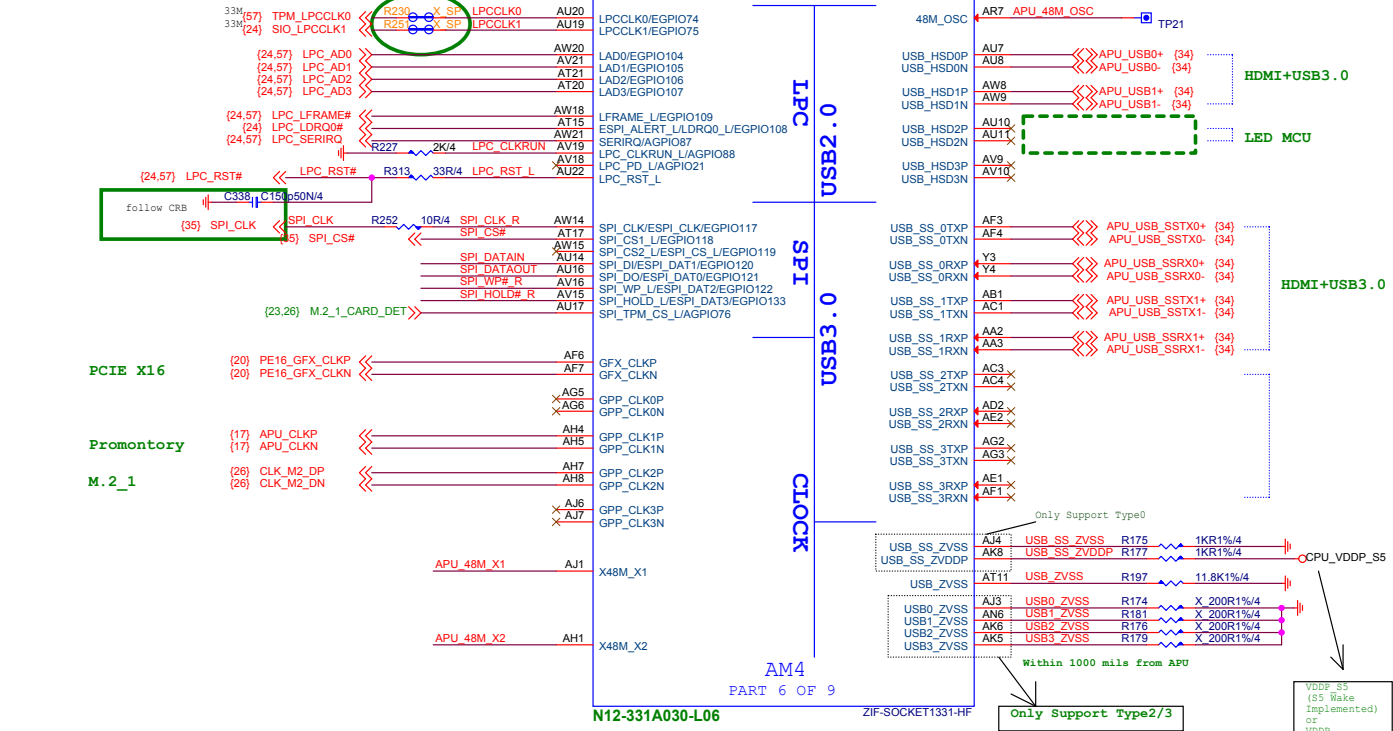
Only supported on TYPE 2

Within 1500 mils from APU
Within 1000 mils from APU



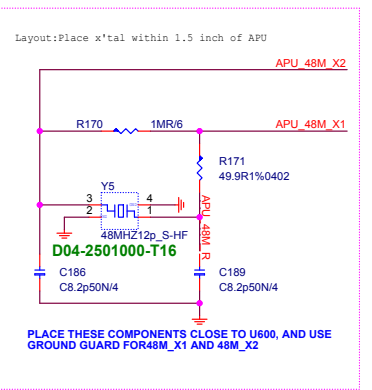


2018/11/30
R230, R251 are changed from 0ohm to copper by cost down

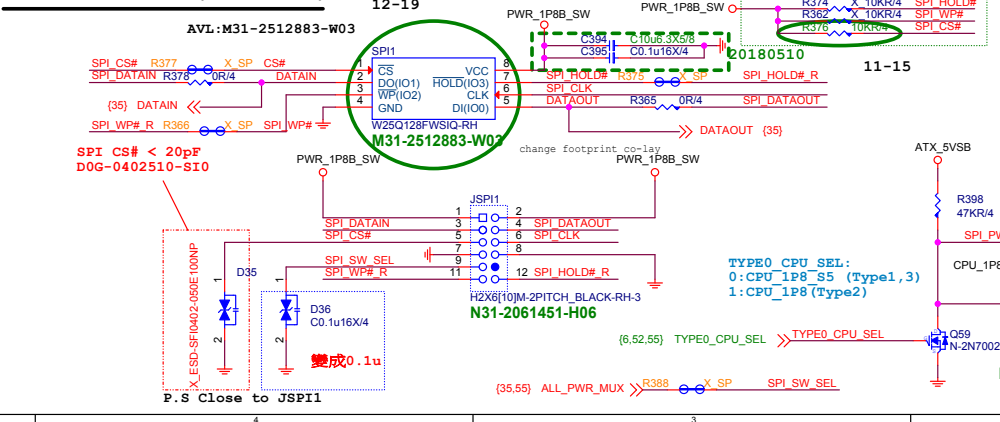


Schematic Cfg	Project
CFG-7C02-**-Arsenal Gaming	V A

2018/11/26
R377, R366, R375, R388 are changed from 0ohm to copper by cost down



SPI ROM(1.8V)



Strapping Options

LPCCLK1				SPI_CLK				LPCCLK0			
PULL HIGH	Configured for Internal clock generator	Use 48Mhz crystal clock and generate both internal and external clocks	LPC device Boot Fail Timer Enabled	(Default)							
PULL LOW	Configured for External clock generator	Use 100Mhz PCIe clock as reference clock and generate internal clocks only	LPC device Boot Fail Timer Disabled				(Default)				

AGPIO3				SIO_LFRAME				SYSREST#			
PULL HIGH	Enhanced Reset logic			SPI ROM				Normal reset mode			
	(Default)			(Default)				(Default)			
PULL LOW	Traditional Reset logic			LPC ROM				short reset mode			

MSI MICRO-STAR INT'L CO.,LTD.

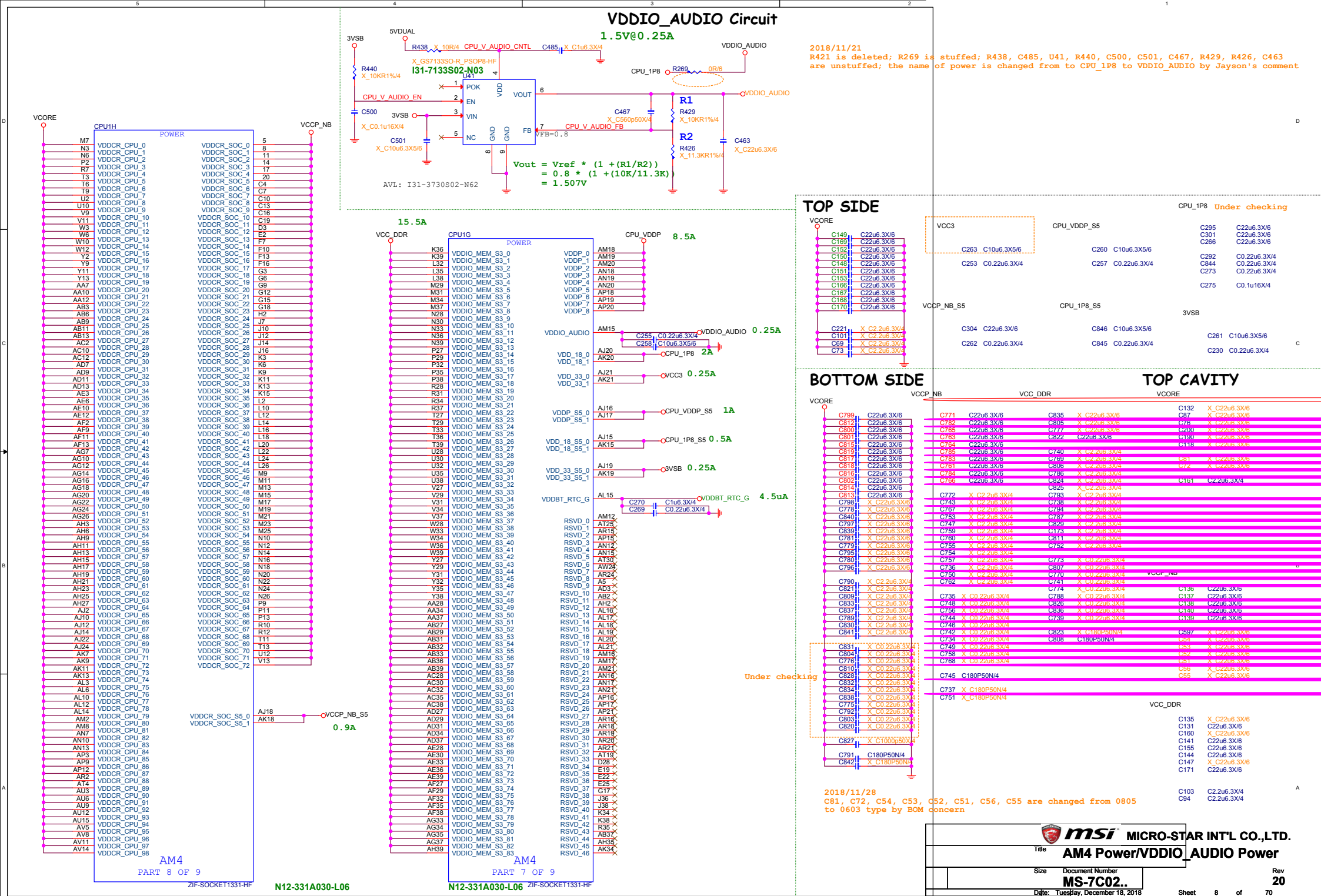
AM4 LPC/SPI/USB/CLK/STRAP

Size Document Number
MS-7C02..

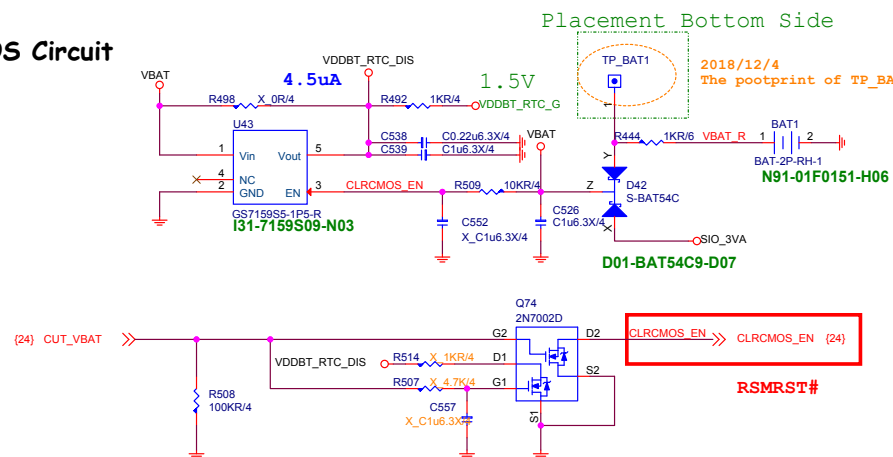
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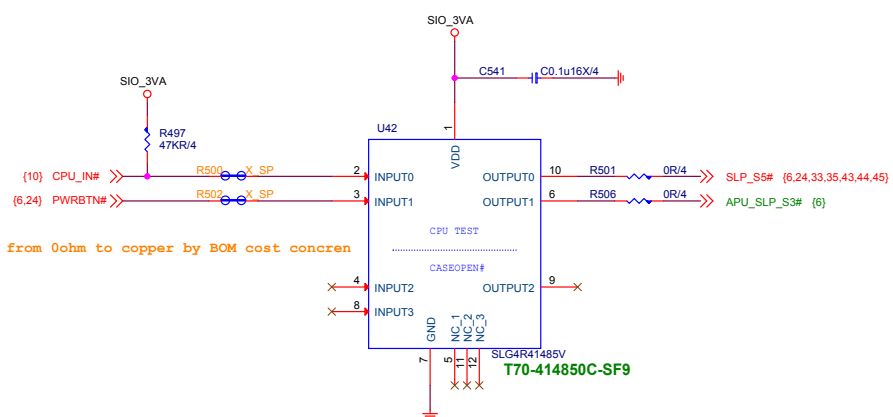
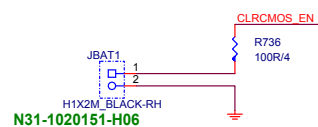


RTC & Clear CMOS Circuit



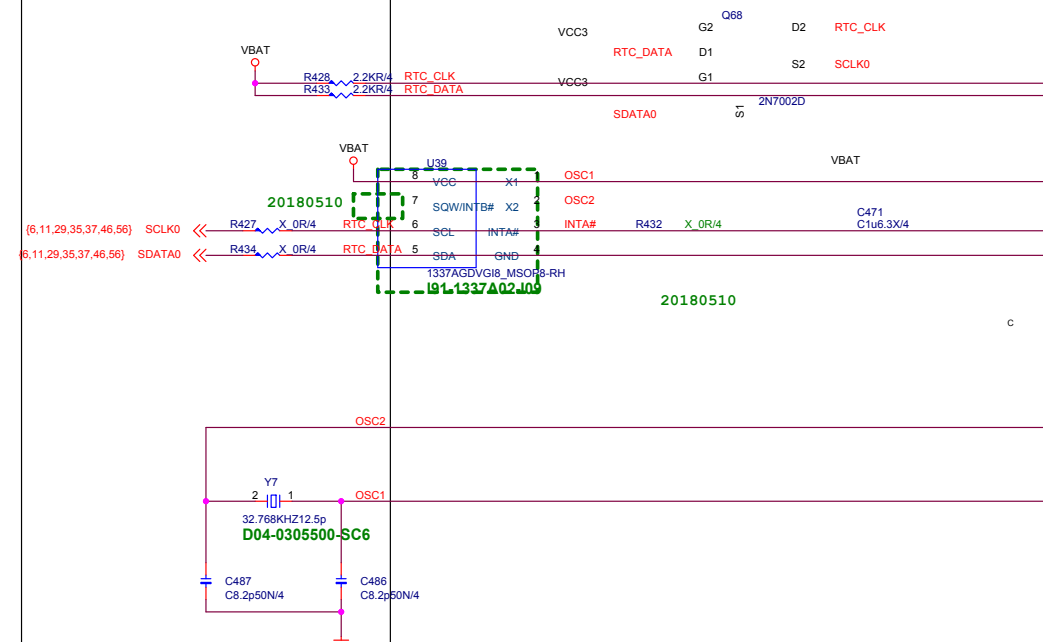
11-17

2018/11/23
R514, R507, C557 are unstuffed by Ryan's comment



2018/11/30
R500, R502 are changed from 0ohm to copper by BOM cost concen

RTC Backup



GND

AM4
PART 9 OF 9

2018/11/26
R200 is are changed from 0ohm to copper by cost down



MICRO-STAR INT'L CO.,LTD.

Title
AM4 GND

Size Document Number
MS-7C02..

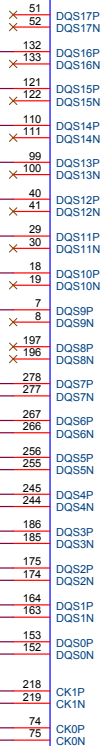
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A1 A2 B1 B2

DIMMA1A



DDR4V-288P_BLACK-RH-21
N13-2880581-L06

2018/11/30

R297, R298 are changed from 0ohm to copper by BOM cost concen

(6,9,29,35,37,46,56) SCLK0 >> SCLK0 R297 X SP SMB_CLK_DIMM >> SMB_CLK_DIMM (12)
(6,9,29,35,37,46,56) SDATA0 >> SDATA0 R298 X SP SMB_DATA_DIMM >> SMB_DATA_DIMM (12)

<< MA_DATA[63..0] (3,11)

56~63

48~55

40~47

32~39

24~31

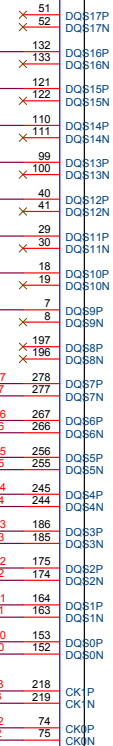
16~23

8~15

0~7

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

DIMMA2A



DDR4V-288P_BLACK-RH-21
N13-2880581-L06

<< MA_DATA[63..0] (3,11)

56~63

48~55

40~47

32~39

24~31

16~23

8~15

0~7

VCC3_SPD

VCC3_SPD_A2A R272 1KR/4

DIMM2 (CHANNEL-A) -A4
ADDRESS = 1:0 [SA1:SA0]

Schematic Cfg		Project		Title		Size		Document Number		Rev	
CFG-7C02-***-Arsenal		V A		DDR4 DIMM CH-A				MS-7C02..		20	
Gaming											

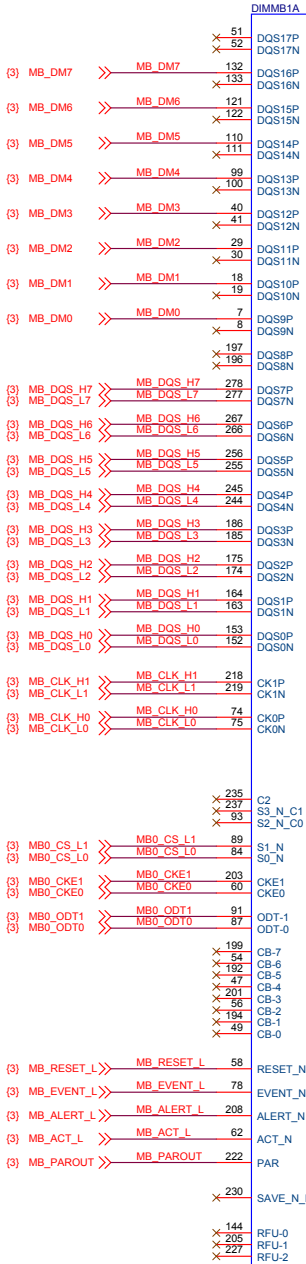
msi MICRO-STAR INT'L CO.,LTD.

MS-7C02..

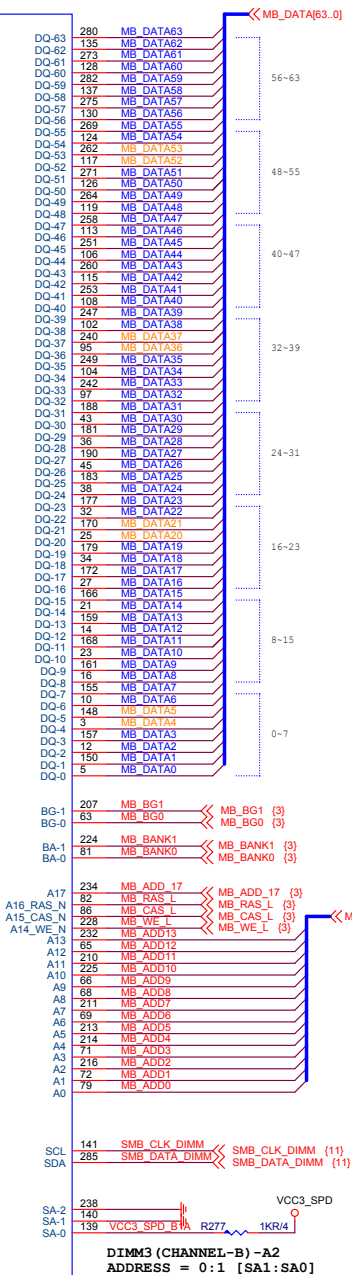
Size Document Number

Rev 20

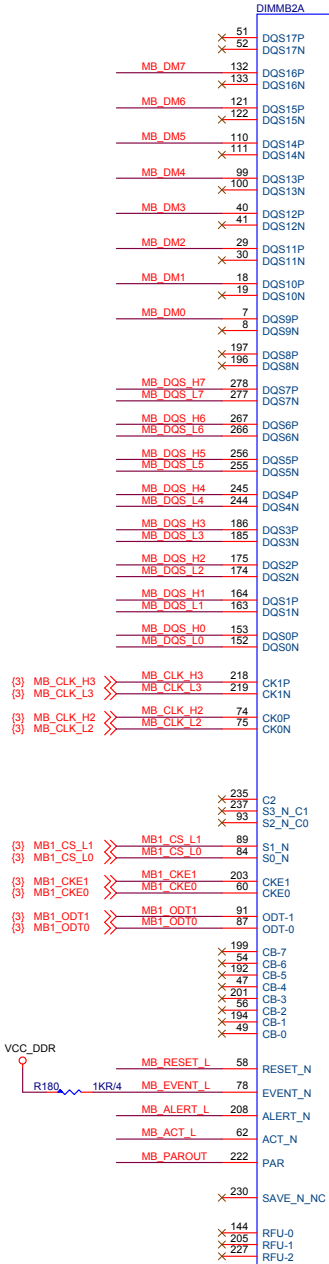
Date: Tuesday, December 18, 2018 Sheet 11 of 70



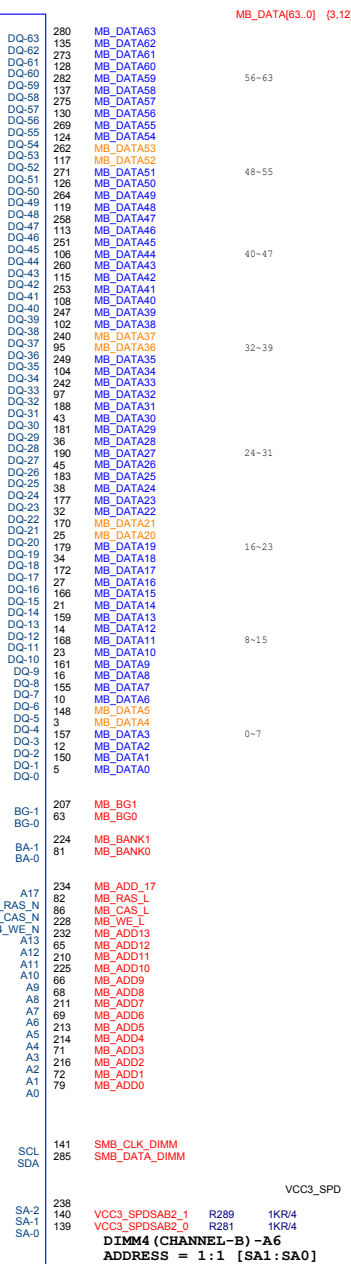
DDRIV-288P_BLACK-RH-21
N13-2880581-L06



DIMM3 (CHANNEL-B) -A2
ADDRESS = 0:1 [SA1:SA0]



DDRIV-288P_BLACK-RH-21
N13-2880581-L06



DIMM4 (CHANNEL-B) -A6
ADDRESS = 1:1 [SA1:SA0]

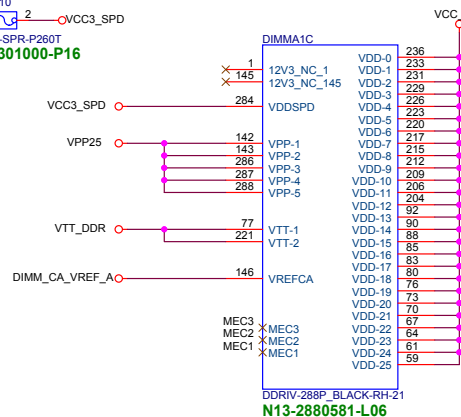
Schematic Cfg		Project		Title	
CFG-7C02***-Arsenal		V A		DDR4 DIMM CH-B	
Gaming				Rev	
				MS-7C02..	
				Date: Tuesday, December 18, 2018	
				Sheet 12 of 70	

msi MICRO-STAR INT'L CO.,LTD.

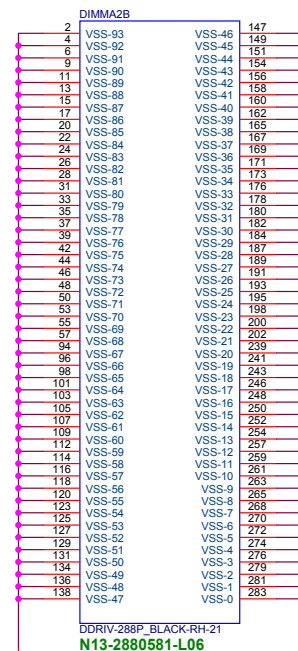
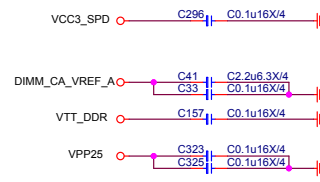
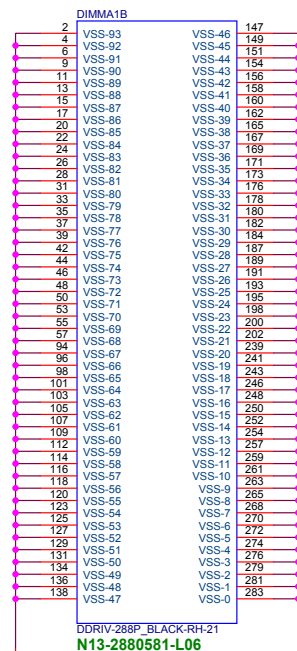
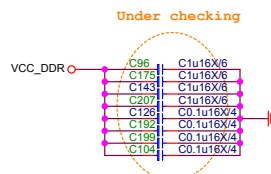
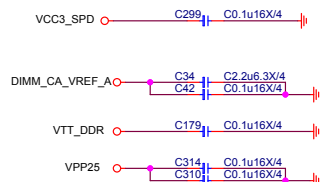
av1:D08-0301100-B07

VCC3 SPD
F10
F-SPR-P260T

D08-0301000-P16

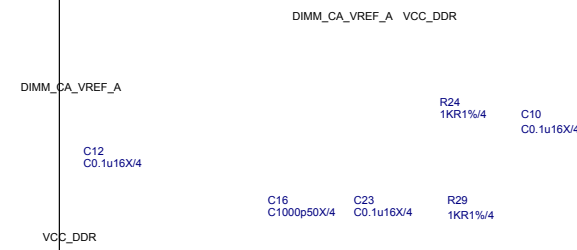


DIMM SLOT PN BY SPEC



DDR VREF

(place resistors close to DIMMs)

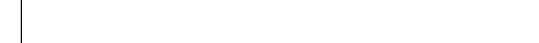
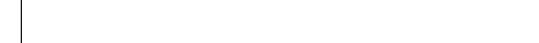
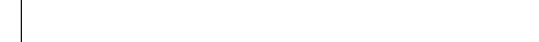
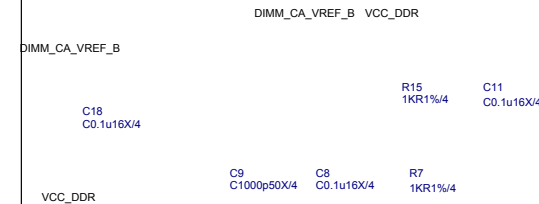


 MICRO-STAR INT'L CO.,LTD.	
Title DDR4-POWER/GND-1	
Size	Document Number
MS-7C02..	
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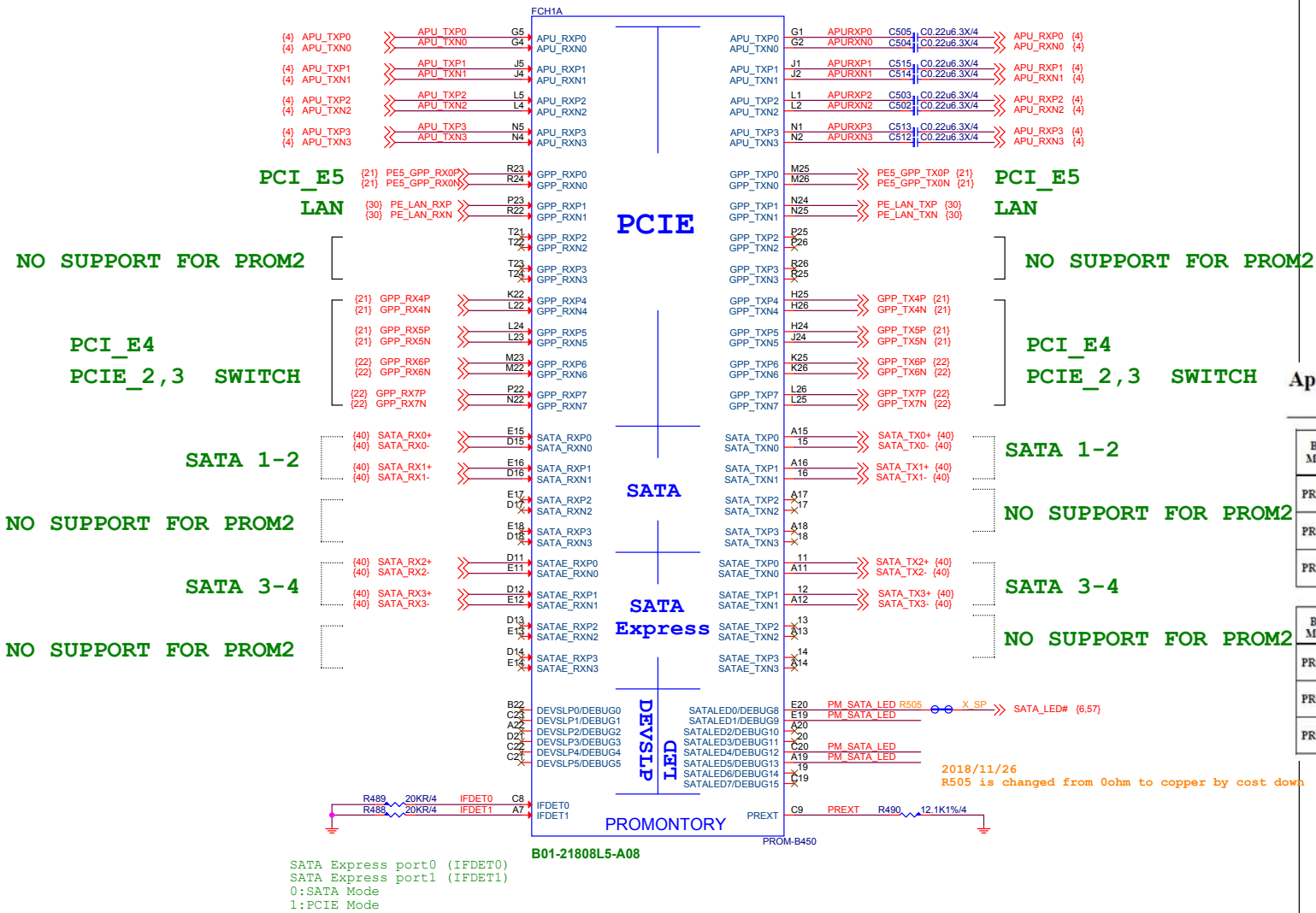
DDR VREF

(place resistors close to DIMMs)



Title		DDR4-POWER/GND-2	
Size	Document Number	MS-7C02..	
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Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2,3不能用
CLK1-3不能用

2018/11/26
R505 is changed from 0ohm to copper by cost down



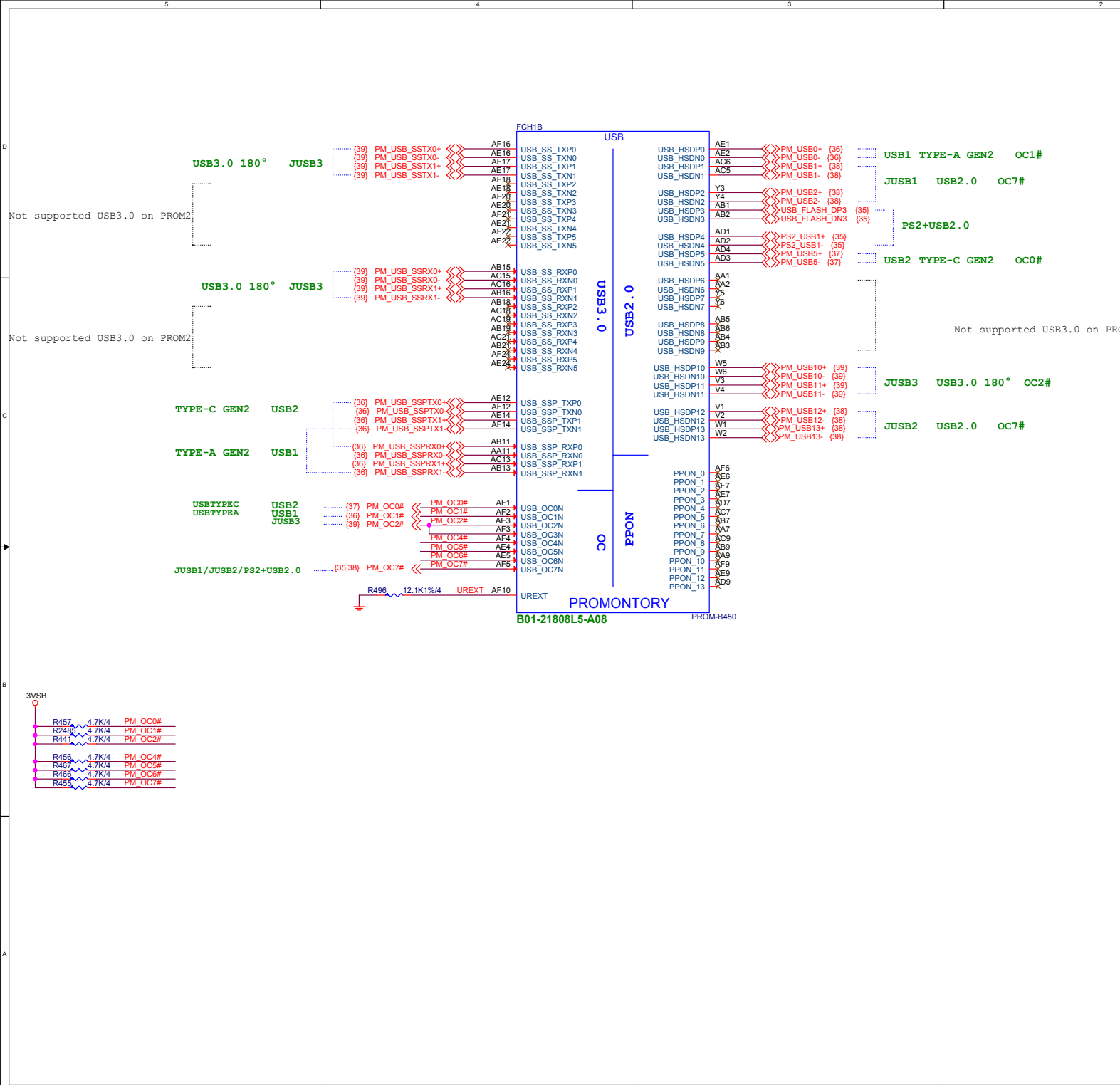
MICRO-STAR INT'L CO.,LTD.
Title Promontory-PCIE/SATA/SATAE

Size Document Number
MS-7C02..

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20

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Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

Appendix C Port Mapping for Different Bus Models

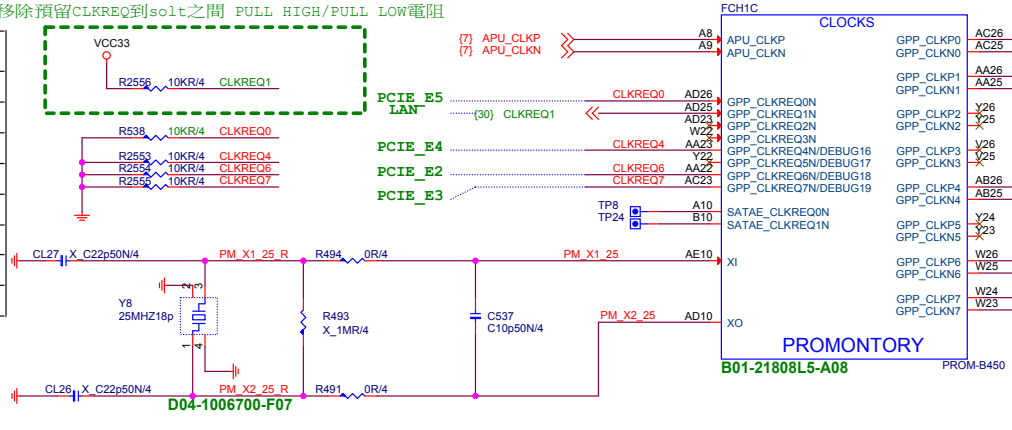
BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~3	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2.3不能用
CLK1-3不能用

移除預留CLKREQ到solt之間 PULL HIGH/PULL LOW電阻

GPP Clock	CLKREQ#
GPP_CLKP/N[0]	GPP_CLKREQ0N
GPP_CLKP/N[1]	GPP_CLKREQ1N
GPP_CLKP/N[2]	GPP_CLKREQ2N
GPP_CLKP/N[3]	GPP_CLKREQ3N
GPP_CLKP/N[4]	GPP_CLKREQ4N
GPP_CLKP/N[5]	GPP_CLKREQ5N
GPP_CLKP/N[6]	GPP_CLKREQ6N
GPP_CLKP/N[7]	GPP_CLKREQ7N

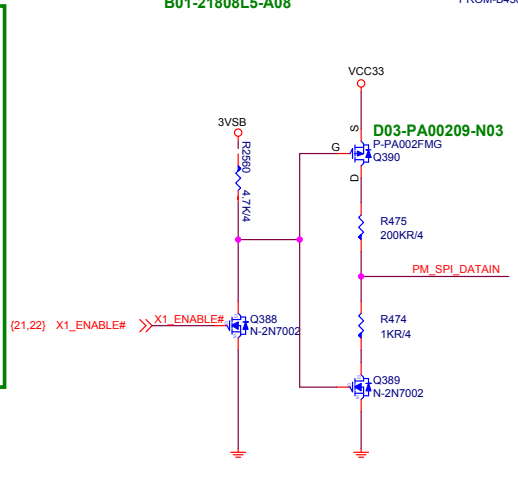
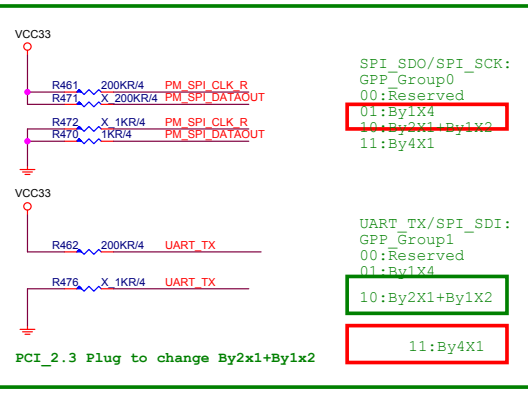
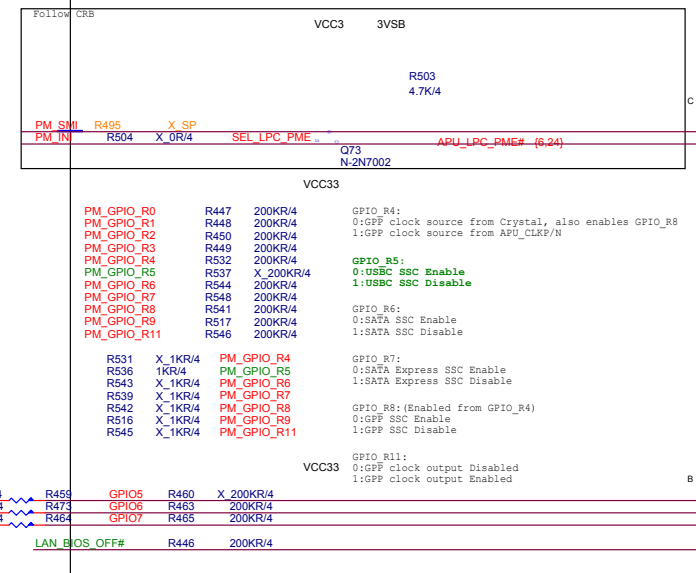
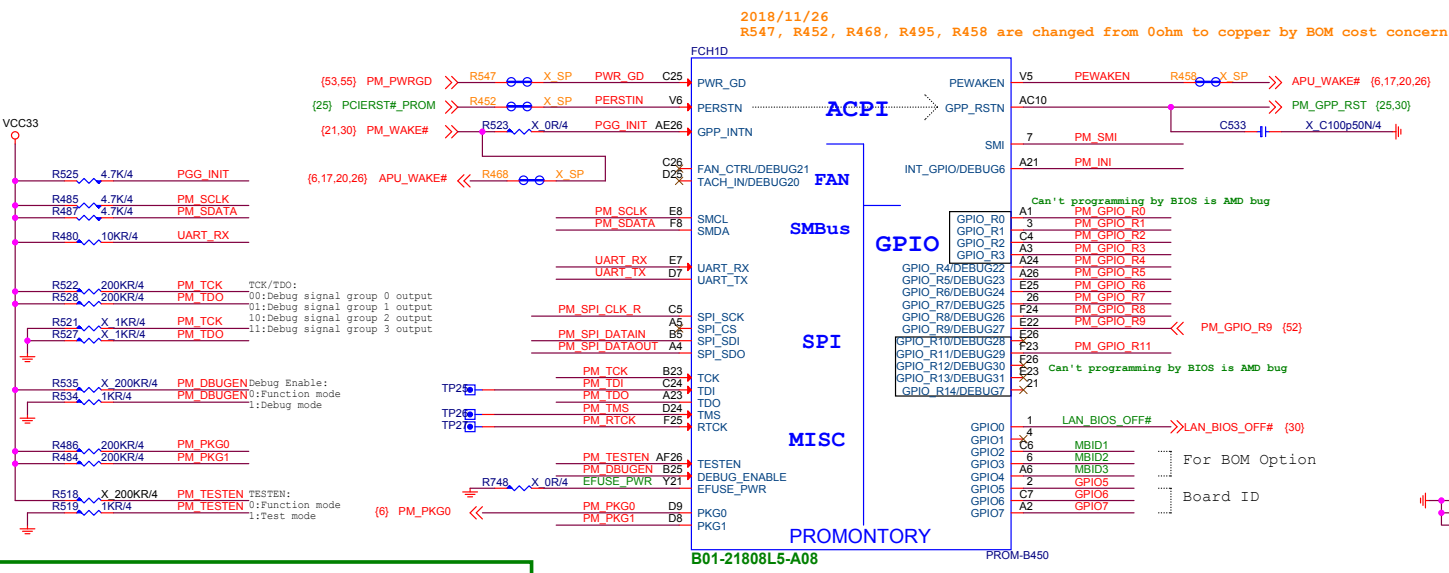


Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0-1	USB_SS Port 0-3	USB_HSD Port0-13	USB_SSP Port0
PROM2	USB_SSP Port0-1	USB_SS Port 0-1	USB_HSD Port0-5 USB_HSD Port10-13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0-5 USB_HSD Port10, 12-13	USB_SSP Port0


BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0-3	SATAE port0-3	GPP lane0-7	CLK0-7
PROM2	SATA port0-1	SATAE port0-1	GPP lane0-1 GPP lane4-7	CLK0-1 CLK4-7
PROM1	SATA port0-1	SATAE port0-1	GPP lane4-7	CLK4-7

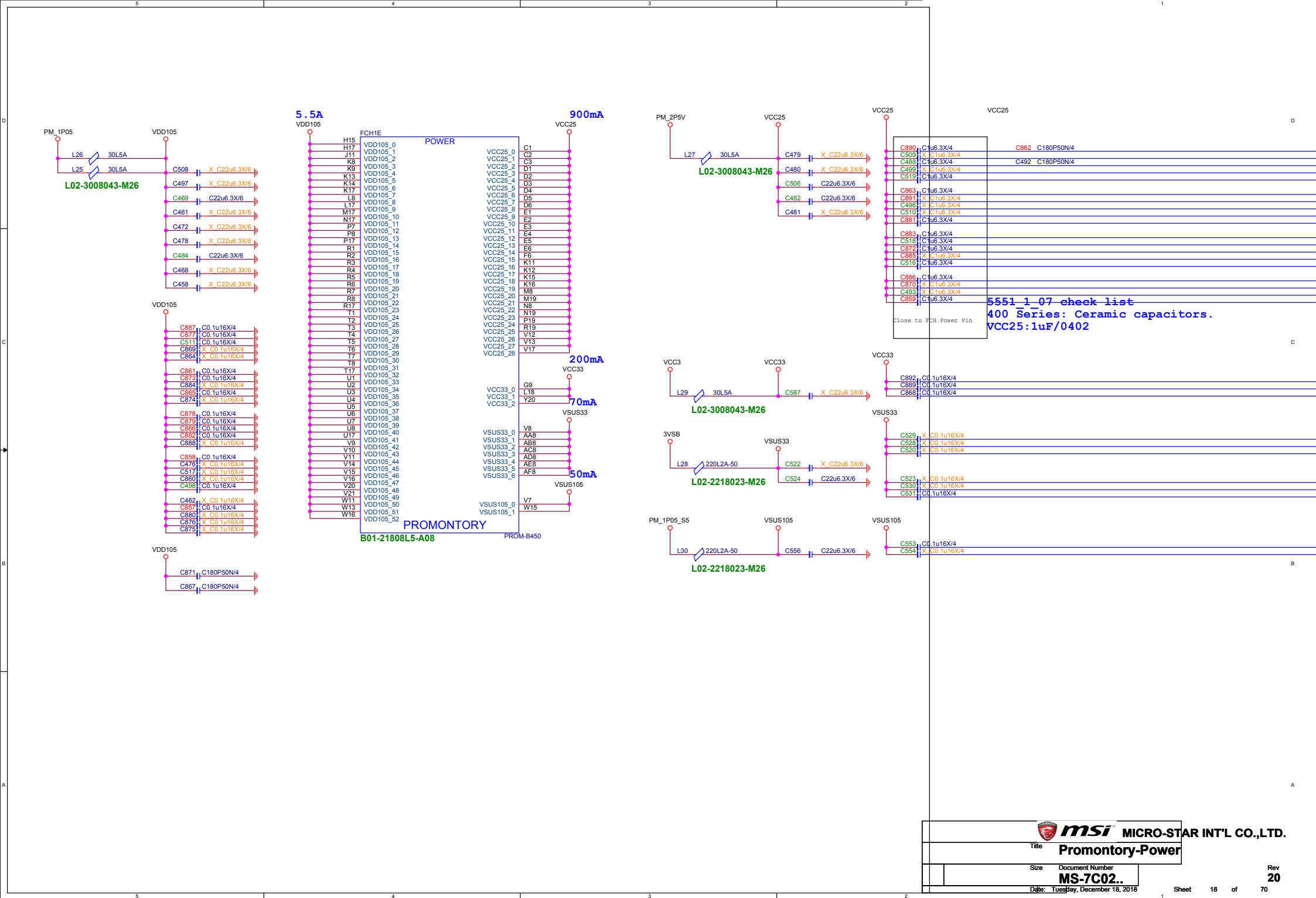
CLK2.3-不能用
CLK1.3-不能用



BOM OPTION

VCC33		MBID1		MBID2		MBID3	
R479	10KR/4	MBID1	R478	X 10KR/4			
R482	X 10KR/4	MBID2	R477	10KR/4			
R483	X 10KR/4	MBID3	R481	10KR/4			
B45-TOMAHAWK 601-7C02-A01							
		1	0	0			
		0	0	0			
		1	1	0			

Schematic Cfg	Project		MICRO-STAR INT'L CO.,LTD.
CFG-7C02-**	V A		
	Title	Promontory-CLK/ACPI/GPIO	
	Size	Document Number	Rev
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GND

PROMONTORY

PROM-B450

B01-21808L5-A08



MICRO-STAR INT'L CO.,LTD.

Title Promontory-GND

Size Document Number
MS-7C02..

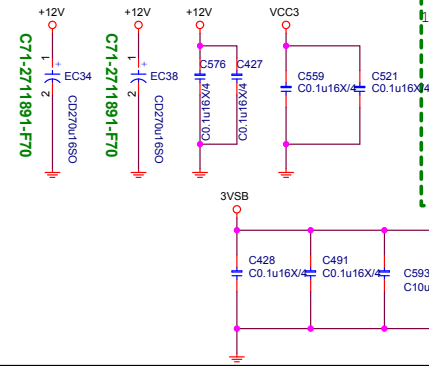
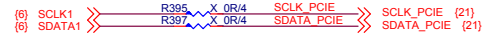
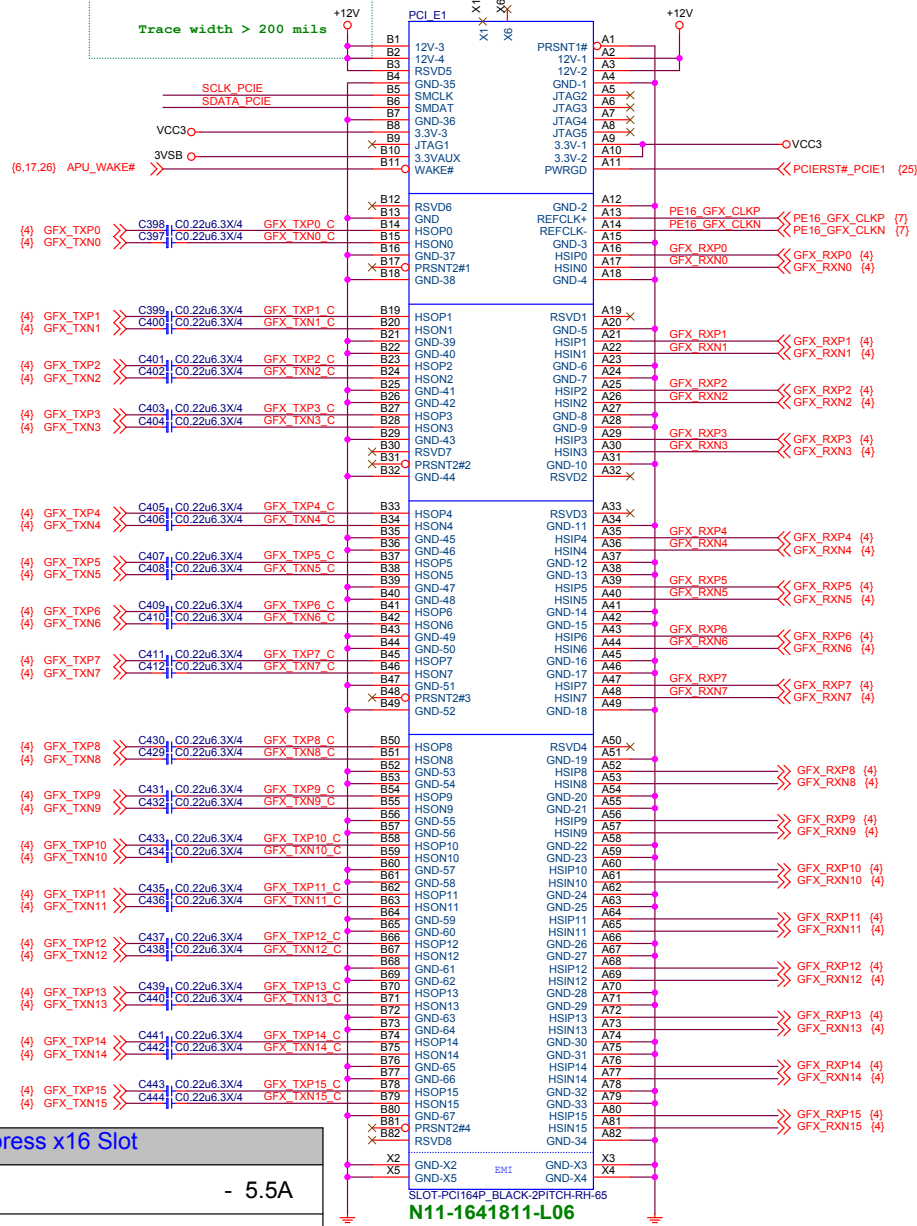
Date: Tuesday, December 18, 2018

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PCI EXPRESS x16 Slot

PCI_E1

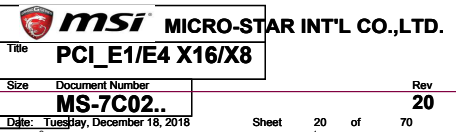


PCI Express x16 Slot

+12V		- 5.5A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

PCI Express x8 Slot

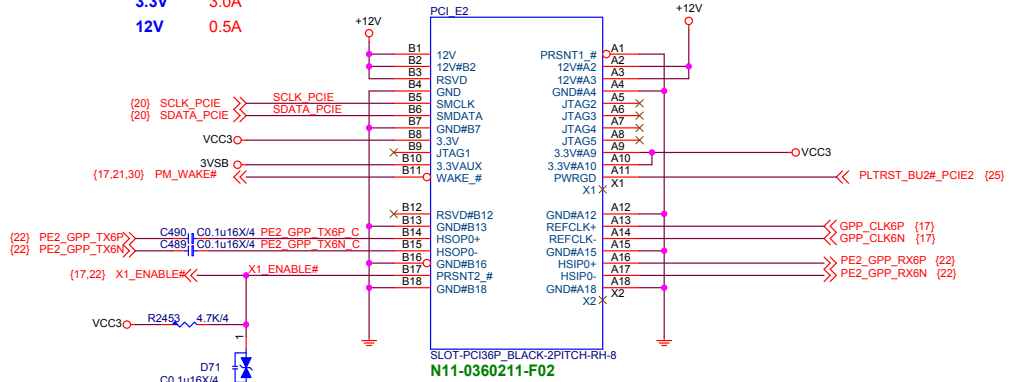
+12V		- 5.5A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA



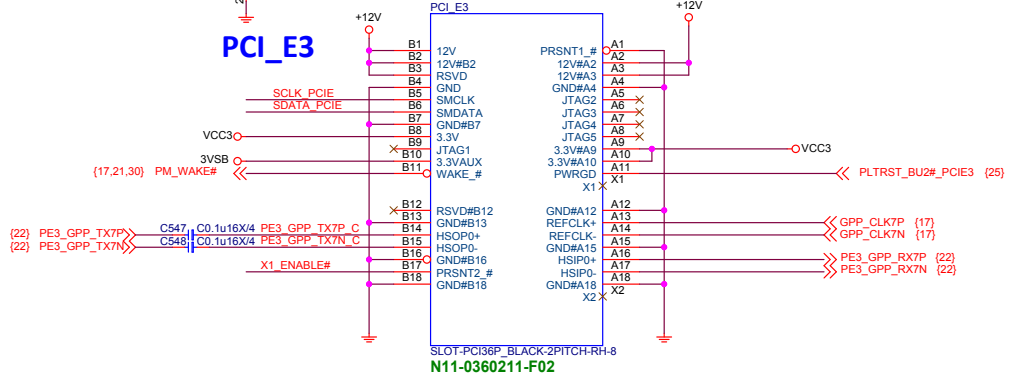
PCIEX1 12V 0.5A
3.3V weak 375mA

PCI_E2

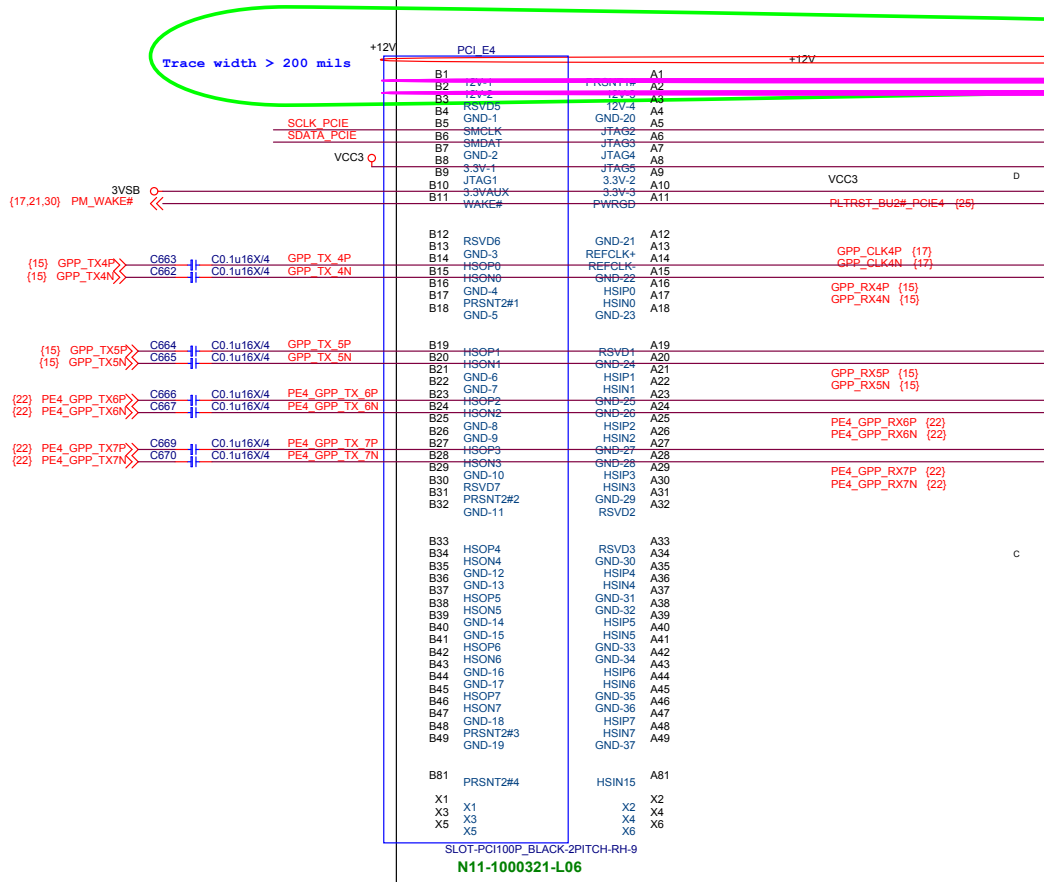
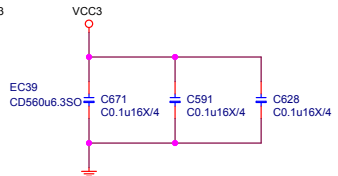
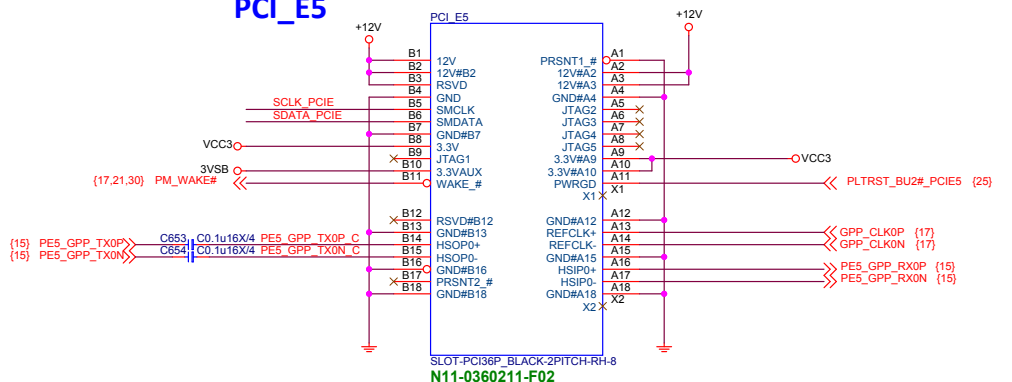
3.3V
12V 3.0A
0.5A



PCI_E3



PCI_E5



PCI Express x4 Slot *1

+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

PCI Express x1 Slot *3

+12V		- 1.5 A
+VCC3		- 9A
+3V3_S5	(wake)	- 1125mA
+3V3_S5	(no wake)	- 60mA

Schematic Cfg

CFG-7C02-***-Arsenal

Gaming

Project

V A

Title

PCI_E2_E3_E5/E4 X1/X4

Size

Document Number

MS-7C02..

Rev

20

Date

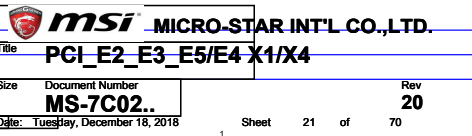
Tuesday, December 18, 2018

Sheet

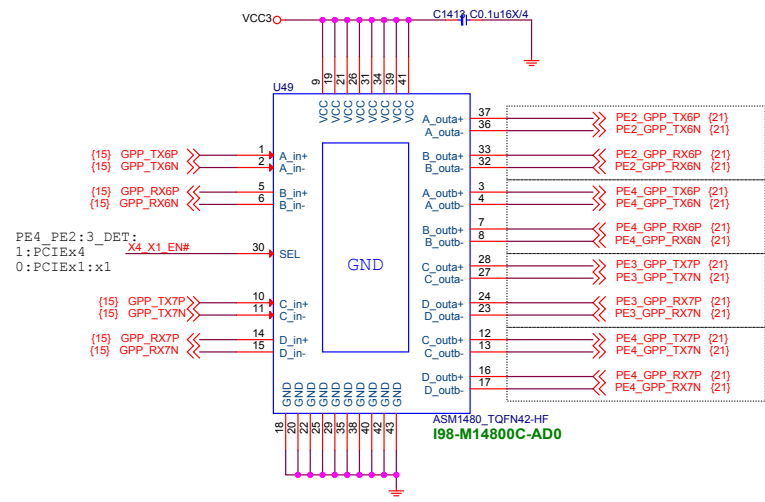
21

of

70



PCI_E4 and PCIE_2 :3 and Switch



PE4 PE2:3_DET:
1:PCIEx4
0:PCIEx1:x1

SEL	Function
L	N_in +/1 to N_out+/-
H	N_in +/1 to N_outb+/-

PCIE_2

PE4

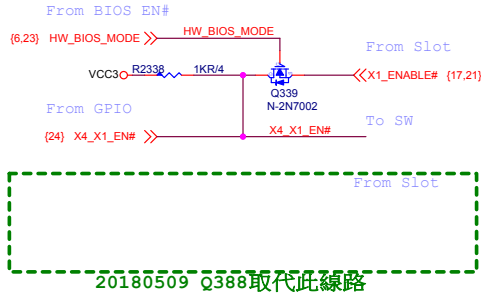
PCIE_3

PE4

UART TX/SPI_SDI:
GPP_Group1
00:Reserved
01:By1x4

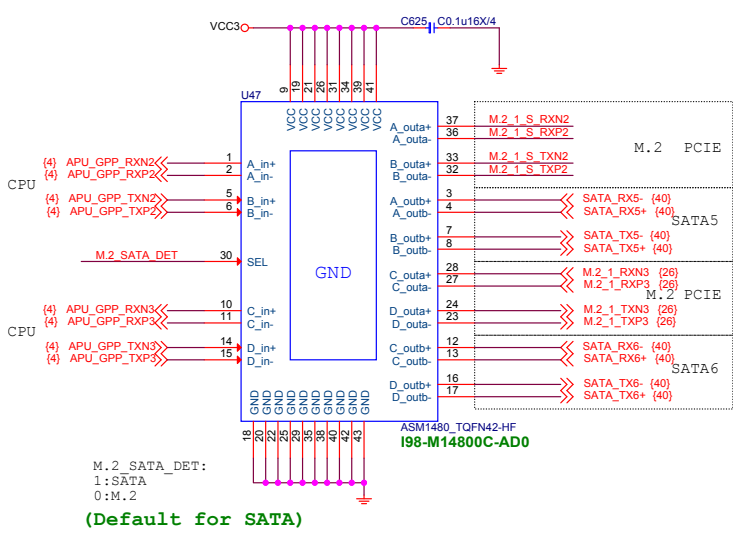
10:By2x1+By1x2
11:By4x1 (def)

PCIE Lanes control circuit

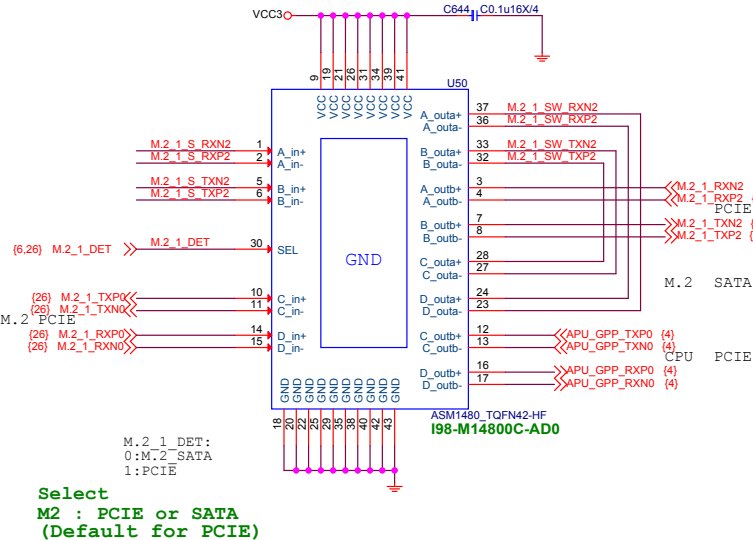


	HW_BIOS_MODE	Q339	Q381	X1_ENABLE#	PM_SPI_DATAIN
Manual x4	L	OFF	OFF	x	11:By4x1 (def)
Manual x2, x1, x1	L	OFF	OFF	L	10:By2x1+By1x2
HW x4	H	ON	ON	H	11:By4X1 (def)
H/W x2,x1,x1	H	ON	ON	L (Stuff PCIE_1)	10:By2x1+By1x2

M2_1 and SATA5 6 Switch



SEL	Function
L	N_in +/1 to N_outa+/-
H	N_in +/1 to N_outb+/-



Select
M2 : PCIE or SATA
(Default for PCIE)

Table 1: M2_1 and SATA5 6 Switch Configuration

	AUTO Mode	SATA CON	M.2 (PCIE)	M.2 (SATA)
HW_BIOS_MODE	1		0	0
M.2_PCIE_CTRL	1		0	0
M.2_1_CARD_DET		1	0	0
M.2_DET		X	1	0

Table 2: M2_1 and SATA5 6 Switch Pin Configuration

Pin	Signal	Function
1	APU_GPP_RXN2	(4) APU_GPP_RXN2
2	APU_GPP_RXP2	(4) APU_GPP_RXP2
5	APU_GPP_TXN2	(4) APU_GPP_TXN2
6	APU_GPP_TXP2	(4) APU_GPP_TXP2
30	M.2 SATA_DET	M.2 SATA_DET
37	M.2_1 S_RXN2	M.2_1 S_RXN2
36	M.2_1 S_RXP2	M.2_1 S_RXP2
33	M.2_1 S_TXN2	M.2_1 S_TXN2
32	M.2_1 S_TXP2	M.2_1 S_TXP2
3	SATA_RX5-	(40) SATA_RX5-
4	SATA_RX5+	(40) SATA_RX5+
7	SATA_TX5-	(40) SATA_TX5-
8	SATA_TX5+	(40) SATA_TX5+
28	M.2_1_RXN3	(26) M.2_1_RXN3
27	M.2_1_RXP3	(26) M.2_1_RXP3
24	M.2_1_TXN3	(26) M.2_1_TXN3
23	M.2_1_TXP3	(26) M.2_1_TXP3
12	SATA_RX6-	(40) SATA_RX6-
13	SATA_RX6+	(40) SATA_RX6+
16	SATA_TX6-	(40) SATA_TX6-
17	SATA_TX6+	(40) SATA_TX6+

Table 3: M2_1 and SATA5 6 Switch Component List

Component	Value	Function
U47	ASM1480, TQFN42-HF	M.2_1 and SATA5 6 Switch
U50	ASM1480, TQFN42-HF	M.2_1 and SATA5 6 Switch
C625	C0.1u16X/4	Capacitor
C644	C0.1u16X/4	Capacitor

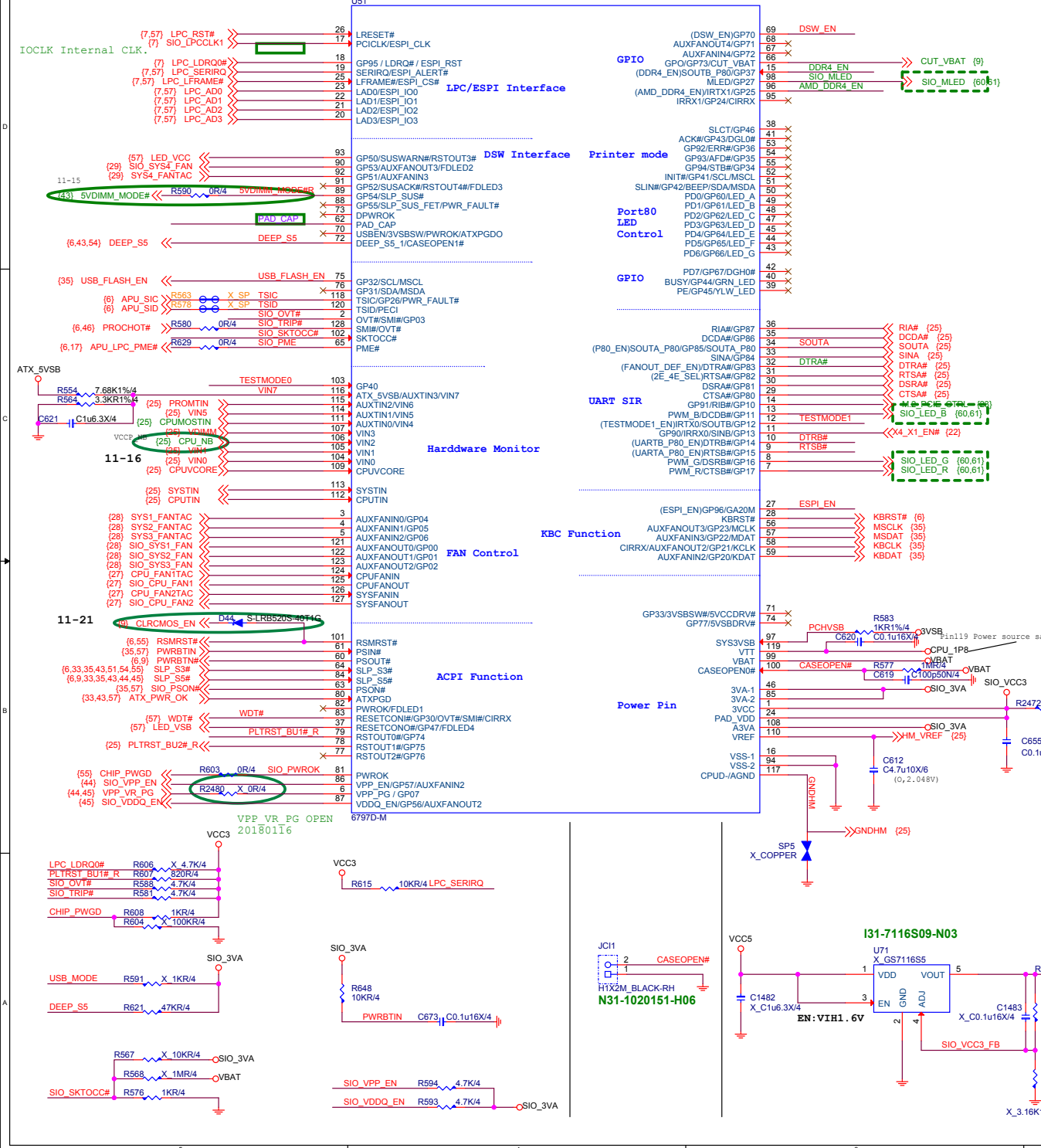
Table 4: M2_1 and SATA5 6 Switch Pin Configuration (Continued)

Pin	Signal	Function
9	VCC3	VCC3
10	M.2_1_DET	M.2_1_DET
11	M.2_1_DET	M.2_1_DET
14	M.2_1_DET	M.2_1_DET
15	M.2_1_DET	M.2_1_DET
12	APU_GPP_TXP0	(4) APU_GPP_TXP0
13	APU_GPP_TXN0	(4) APU_GPP_TXN0
16	APU_GPP_RXP0	(4) APU_GPP_RXP0
17	APU_GPP_RXN0	(4) APU_GPP_RXN0

Table 5: M2_1 and SATA5 6 Switch Pin Configuration (Continued)

Pin	Signal	Function
37	M.2_1 SW_RXN2	M.2_1 SW_RXN2
36	M.2_1 SW_RXP2	M.2_1 SW_RXP2
33	M.2_1 SW_TXN2	M.2_1 SW_TXN2
32	M.2_1 SW_TXP2	M.2_1 SW_TXP2
3	M.2_1_RXN2	(26) M.2_1_RXN2
4	M.2_1_RXP2	(26) M.2_1_RXP2
7	M.2_1_TXN2	(26) M.2_1_TXN2
8	M.2_1_TXP2	(26) M.2_1_TXP2

2018/11/26
R563, R578 are changed from 0ohm to copper by cost down

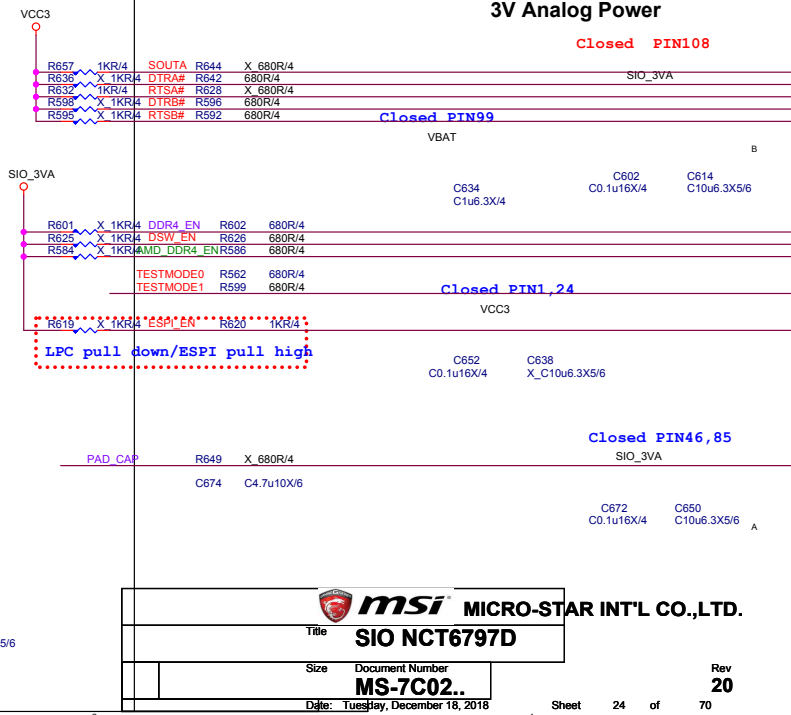


POWER ON STRAPPING PIN FOR NCT6797/6795					
PIN 6797/6795 NAME		Circuit NAME		0	1
				Strap Point	
9	UARTA_P80_EN	RTSB#	DISABLE	ENABLE	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE	ENABLE	LRESET
12	TESTMODE1_EN	TESTMODE1_EN	DISABLE	ENABLE	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	ESPI_EN	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	6795 TESTMODE_EN	6795 WDT#	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMRST
	6797 GP40	6797 WDT#			

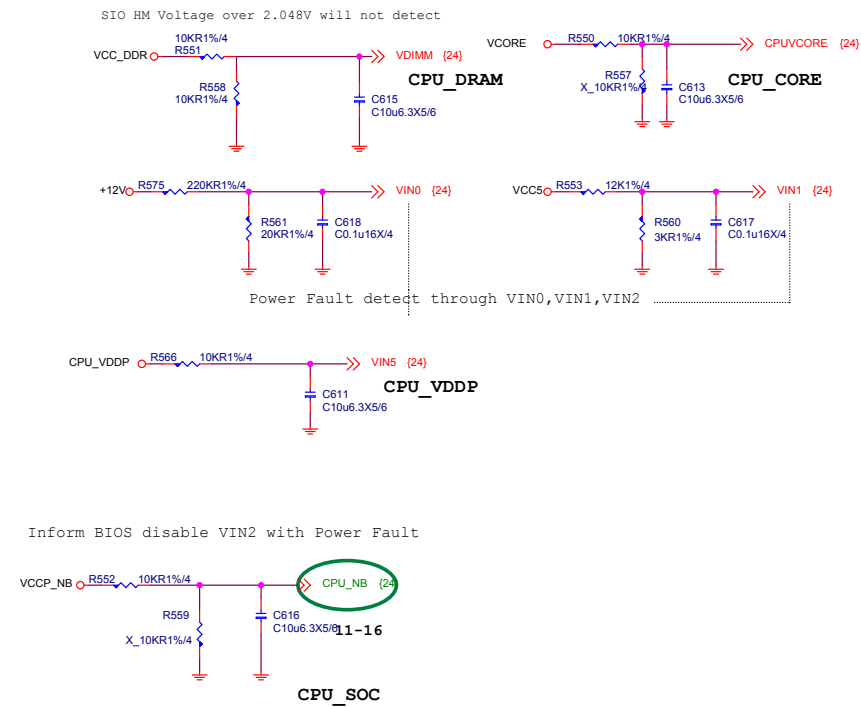
Note:
If PIN34 strapping low, BIOS must programming LPT or GPIO

DTRA# high FAN 100% LOW FAN 50%

3V Analog Power

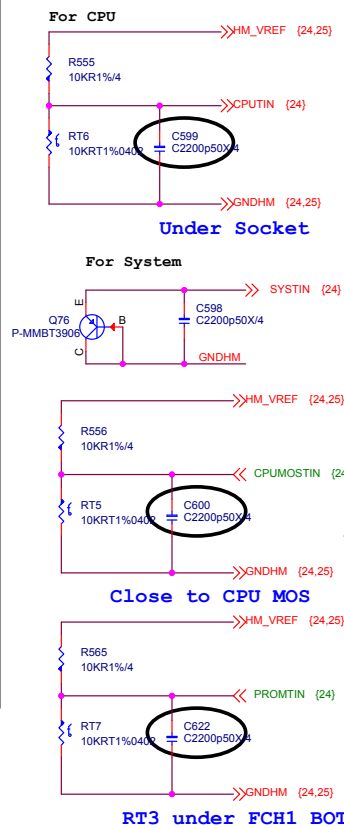


HW Monitor - Voltage

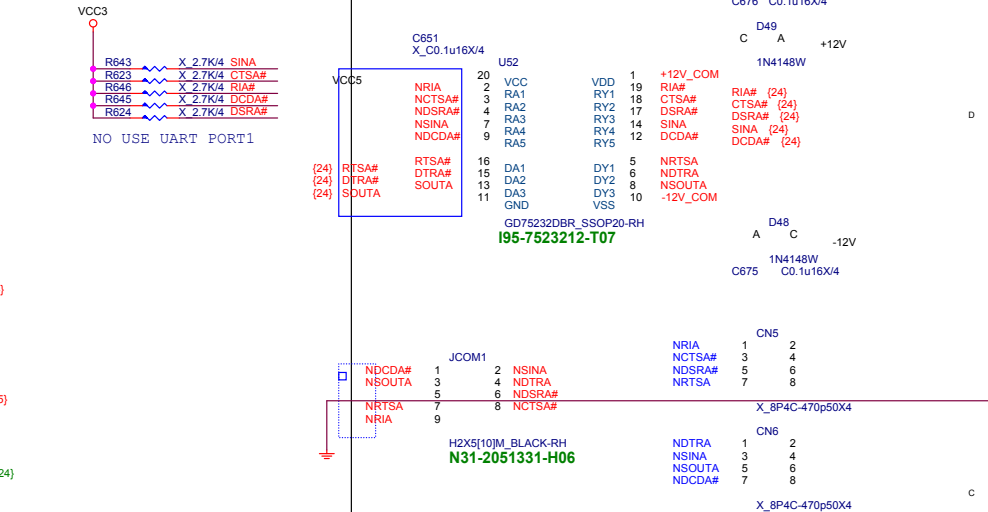


PARALLAL PORT

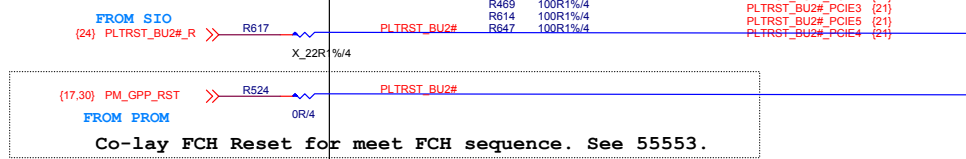
TEMP SENSOR



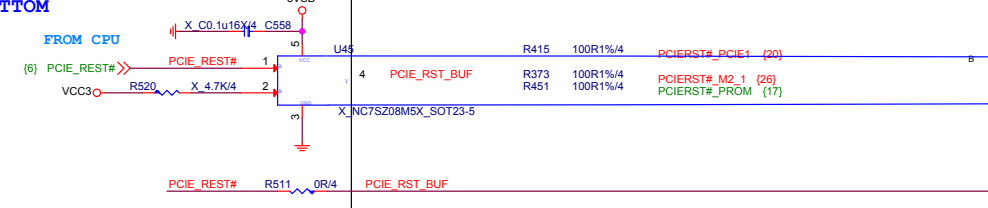
COM PORT



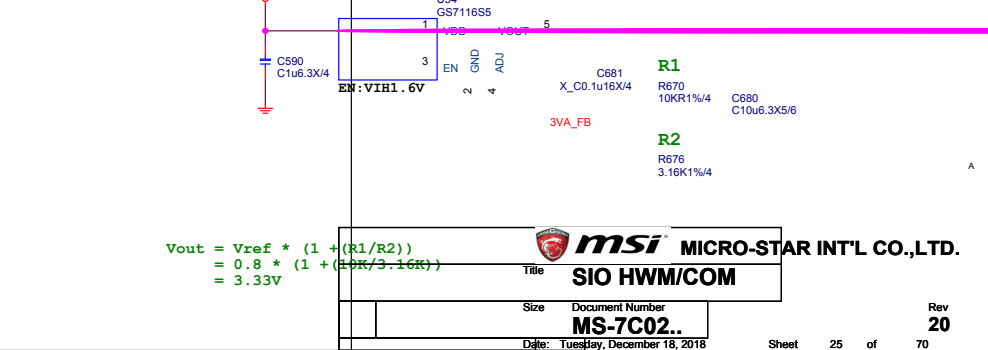
PROM RESET



CPU RESET



SIO_3VA



$$V_{out} = V_{ref} * (1 + (R1/R2))$$
$$= 0.8 * (1 + (10K/3.16K))$$
$$= 3.33V$$

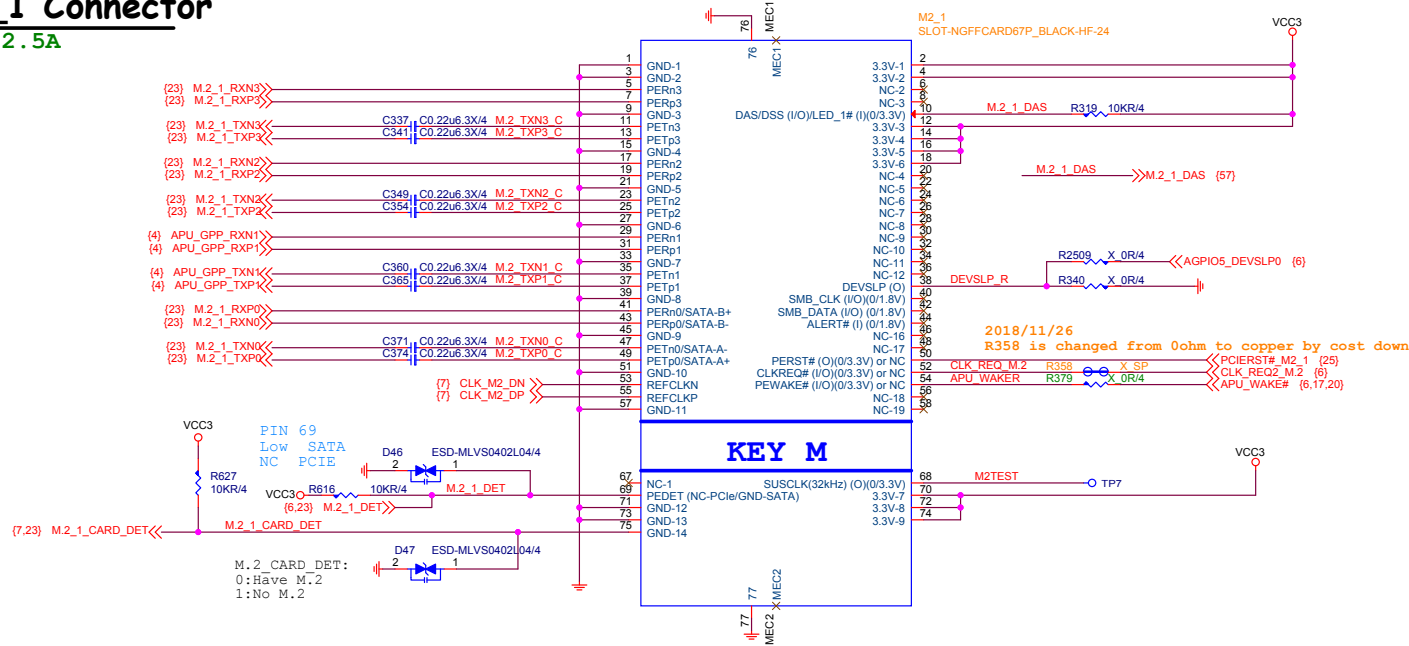
M.2_1 Connector

3.3V@2.5A

2018/11/28

M2_1 is updated Capture's library by Eric's comment

3.3V@2.5A



VCC3

C361 C362 C334 C346 C324 C390 C387 C340
C10u6.3X5/6 C0.1u16X/4 X_C0.1u16X/4 X_C0.1u16X/4 X_C0.1u16X/4 C0.1u16X/4

SCREW1

SCREW

STANDOFF
E2B-7984020-A89

H5 <HP-BOM> H6 <HP-BOM> H7 <HP-BOM> H8 <HP-BOM>

1 Screw E2B-7B05010 1 Screw E2B-7B05010 1 Screw E2B-7B05010 1 Screw E2B-7B05010

Footprint: H_R240D173_BR189_PT

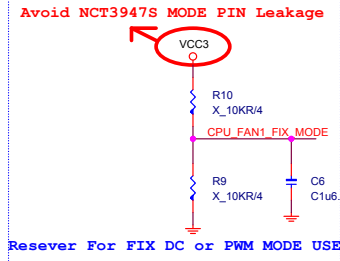
E2B-7B05010-A89 E2B-7B05010-A89
E2B-7B05010-A89 E2B-7B05010-A89

Schematic Cfg	Project	msi	MICRO-STAR INT'L CO.,LTD.
CFG-7C02-*-*-Arsenal	V A	Title	M.2_1
Gaming		Size	Document Number
		MS-7C02..	Rev
		Date: Tuesday, December 18, 2018	20
		Sheet	26 of 70

TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

- 1.Mode GPIO BIOS can switch PWM/DC MODE
- 2.FM:BIOS can read FAN PWM/DC MODE

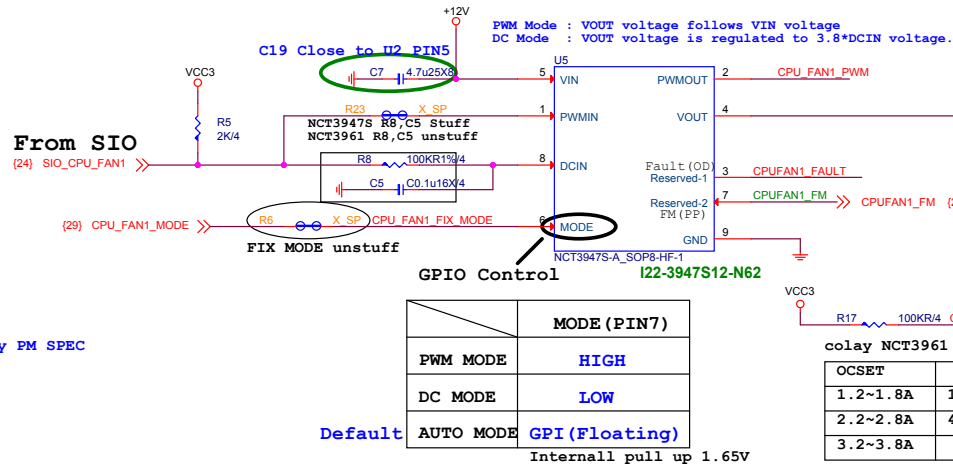
CPU_FAN1



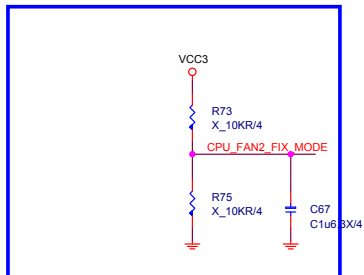
2018/11/30

R6, R23 are changed from 0ohm to copper by BOM cost concen

If C19 place high thermal area,You can change X7R cap.



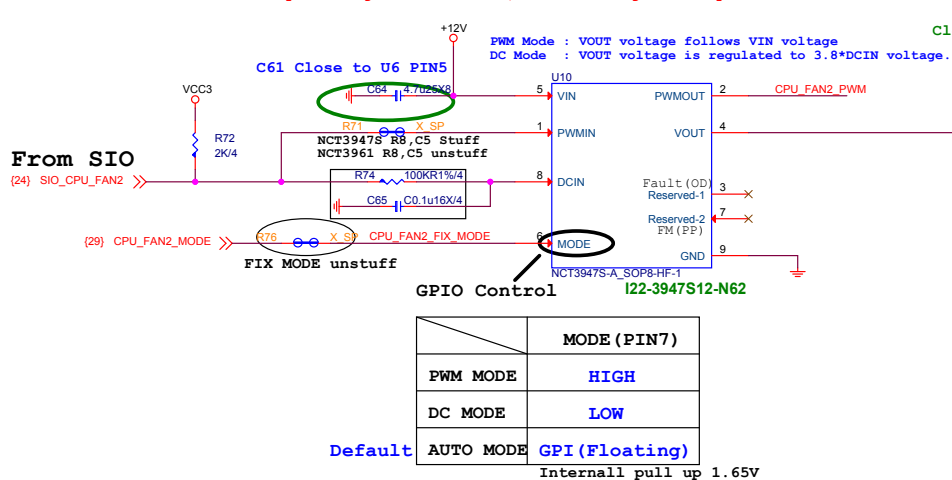
PUMP_FAN1



2018/11/30

R71, R76 are changed from 0ohm to copper by BOM cost concen

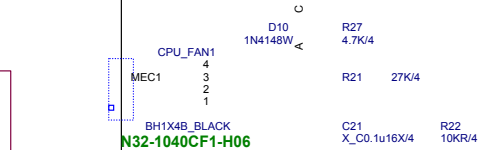
If C61 place high thermal area,You can change X7R cap.



CPU_FAN1_PWM R32 100R/4 +12V >40mil

C29 X_C0.1u16X/4 C20 C0.1u16X/4

Close to FAN Connector



CPUFAN PWR >40mil

C26 C22u16X/5/8 C40 C0.1u16X/4

Close to FAN Connector

colay NCT3961

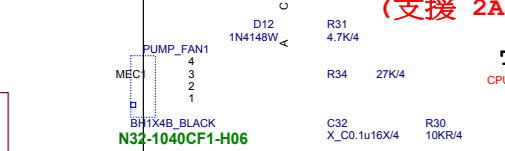
OCSET	R1	default
1.2~1.8A	100K	
2.2~2.8A	49.9K	
3.2~3.8A	10K	

OC SET By PM SPEC
20170428

CPU_FAN2_PWM R70 100R/4 +12V >80mil

C59 X_C0.1u16X/4 C66 C0.1u16X/4

Close to FAN Connector



CPUFAN PWR >40mil

C62 C22u16X/5/8 C60 C0.1u16X/4

Close to FAN Connector

msi MICRO-STAR INT'L CO.,LTD.

Title CPU_FAN1/PUMP_FAN1

Size Document Number
MS-7C02..

Date: Tuesday, December 18, 2018

Rev 20
Sheet 27 of 70

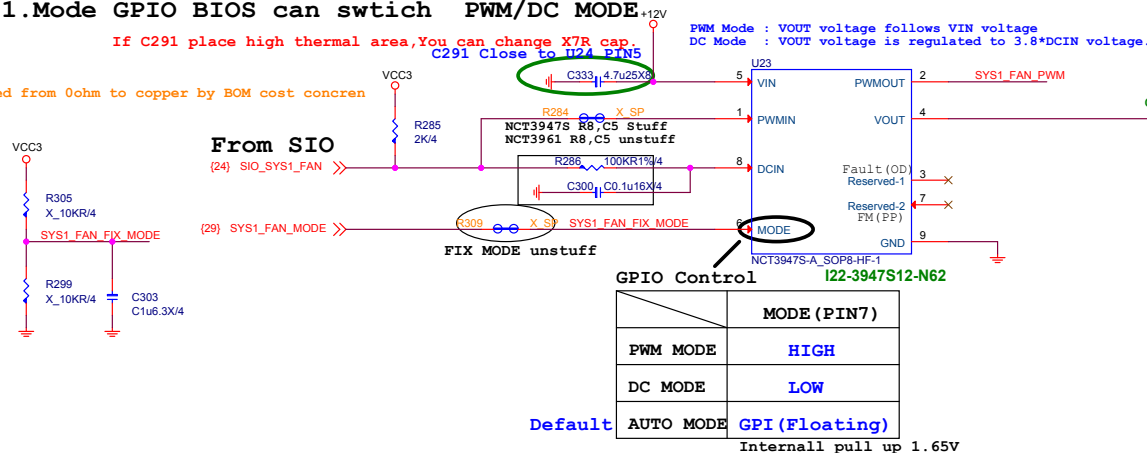
SYSFAN

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE

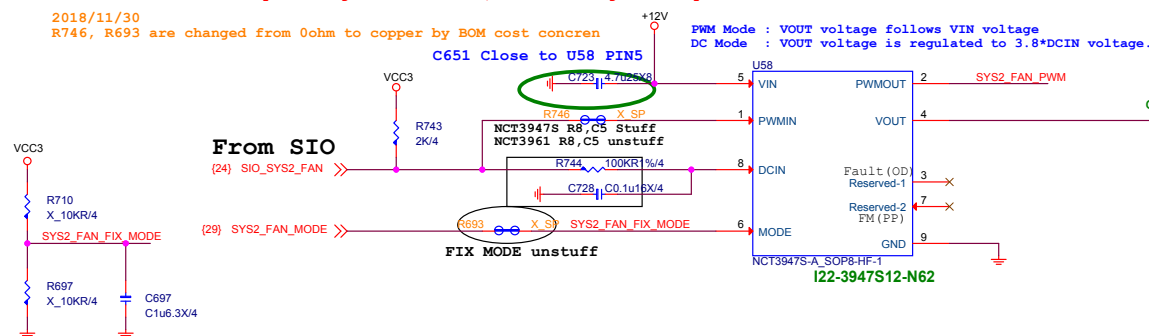
If C291 place high thermal area,You can change X7R cap.
C291 Close to U24 PIN5

2018/11/30
R284, R309 are changed from 0ohm to copper by BOM cost concen

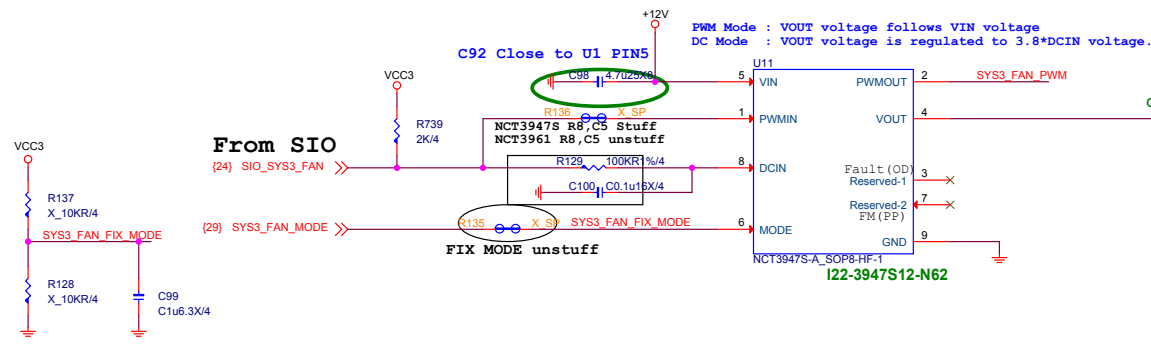


If C651 place high thermal area,You can change X7R cap.

2018/11/30
R746, R693 are changed from 0ohm to copper by BOM cost concen



2018/11/30
R135, R136 are changed from 0ohm to copper by BOM cost concen
If C92 place high thermal area,You can change X7R cap.



SYS3_FAN_PWM R80 100R/4 +12V >40mil

C70 X_C0.1u16X/4 C106 C0.1u16X/4

Close to FAN Connector

SYS3_FAN_PWR

CPUFAN_PWR >40mil

Close to FAN Connector

SYS3_FAN_PWR

CPUFAN_PWR >40mil

Close to FAN Connector

SYS3_FAN_PWR

CPUFAN_PWR >40mil

Close to FAN Connector

SYS3_FAN_PWR

CPUFAN_PWR >40mil

Close to FAN Connector

SYS3_FAN_PWR

CPUFAN_PWR >40mil

Close to FAN Connector

SYS3_FAN_PWR

CPUFAN_PWR >40mil

Close to FAN Connector

SYS3_FAN_PWR

msi MICRO-STAR INT'L CO.,LTD.

Title SYS_FAN1-3

Size Document Number MS-7C02..

Date: Tuesday, December 18, 2018

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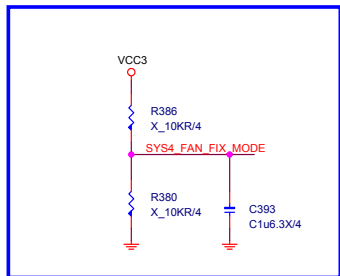
Rev 20

SYSFAN 4

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

If C598 place high thermal area, You can change X7R cap.

2018/11/30
R383, R387 are changed from 0ohm to copper by BOM cost concen



From SIO

(24) SIO_SYS4_FAN

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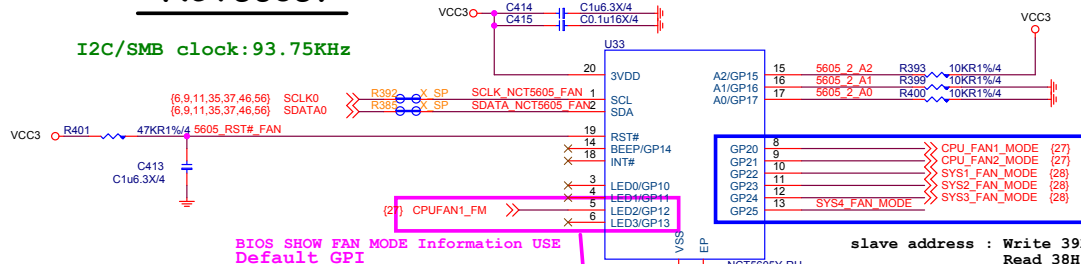
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(24) SIO_SYS4_FAN

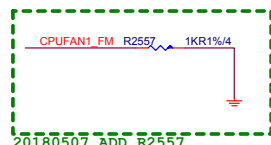
(24) SIO_SYS4_FAN

NCT5605Y

I2C/SMB clock: 93.75KHz



BIOS SHOW FAN MODE Information USE
Default GPI



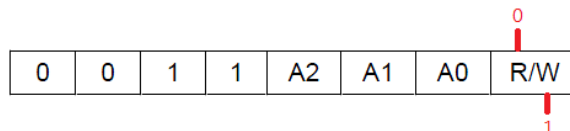
By PM Define FAN name

SHOW FAN MODE USE	FAN
GP12	CPUFAN1
GP13	CPUFAN2 PUMPFAN

1. GENERAL DESCRIPTION

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power-on reset or from external reset.

NCT5605Y SMBus™ Address is:



By PM Define FAN name

FAN USE	MODE	FAN
GP20	CPUFAN1	
GP21	CPUFAN2 PUMPFAN	B
GP22	SYSFAN1	
GP23	SYSFAN2	
GP24	SYSFAN3	
GP25	SYSFAN4	

RTL8111H Giga LAN

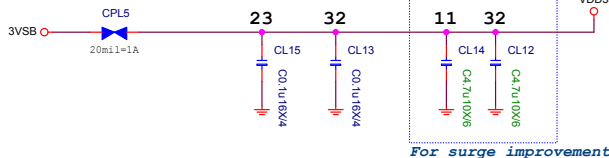
VDD33
RL14 X 1KR/4 LAN_WAKE#

Remove pull-up R if R existence on motherboard
(or SB has internal pull-up R).

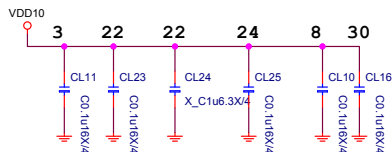
VCC3
RL16 1KR1%/4
RL13 15K1%/4 ISOLATEB

2018/11/26
RL15 is changed from 0ohm to copper by cost down

VDD33@65mA



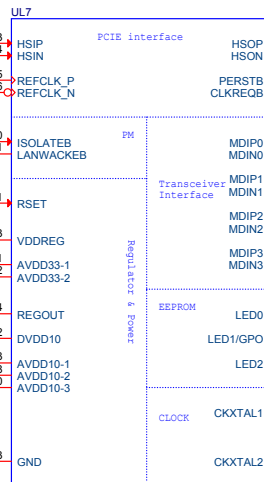
VDD10@150mA



Pull-up resistor RL9 required to either
3.3V suspend or core rail depending on
the power well of the PCH input CLKREQ# buffer.

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

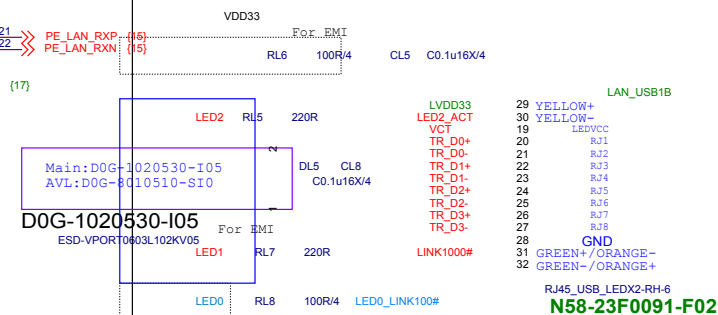


B06-08111CC-R09

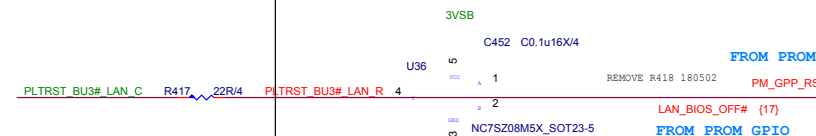
Pin33: 4 via from top layer to GND layer
and make the via at the center of IC.

PIN19:
AMD platform connect to PCIE_RST#,
don't connect to A-RST#.
INTEL platform connect to PLT_RST#.

LAN Connector

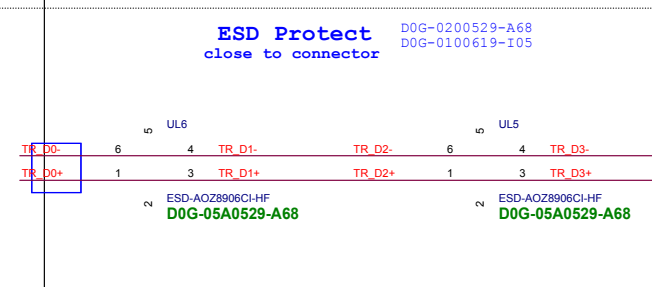


D04-1000201-F07



ESD Protect
close to connector

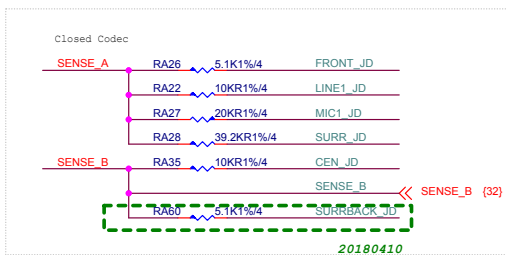
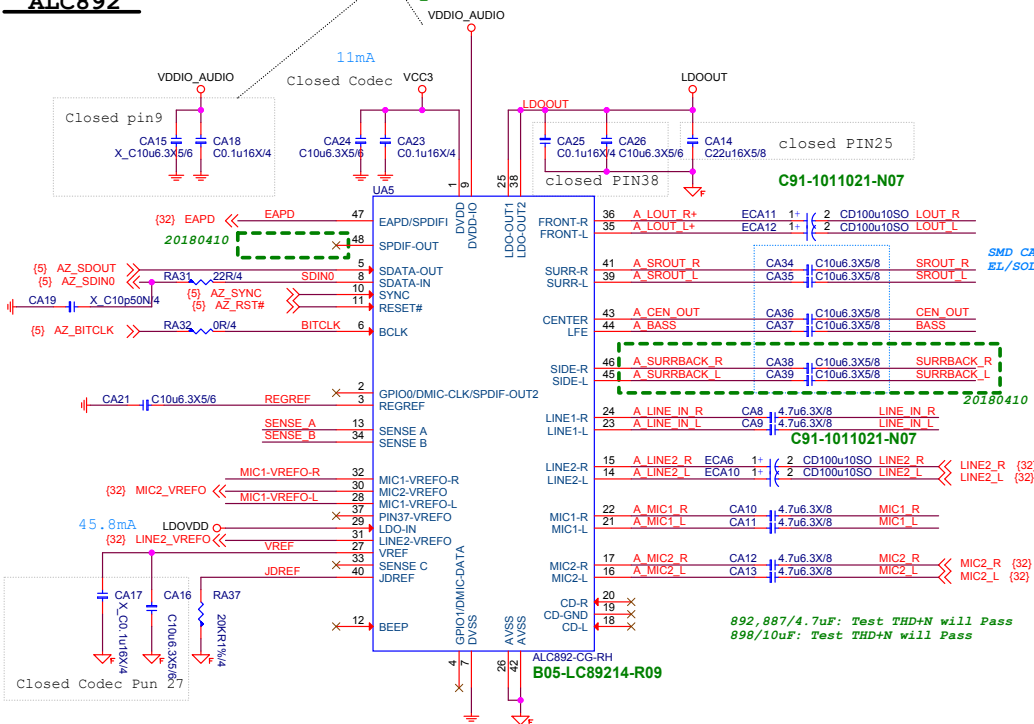
D0G-0200529-A68
D0G-0100619-I05



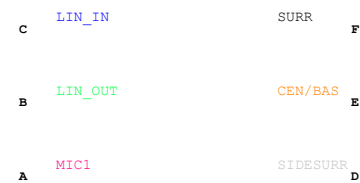
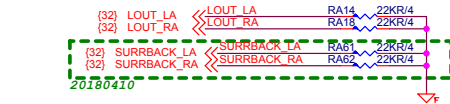
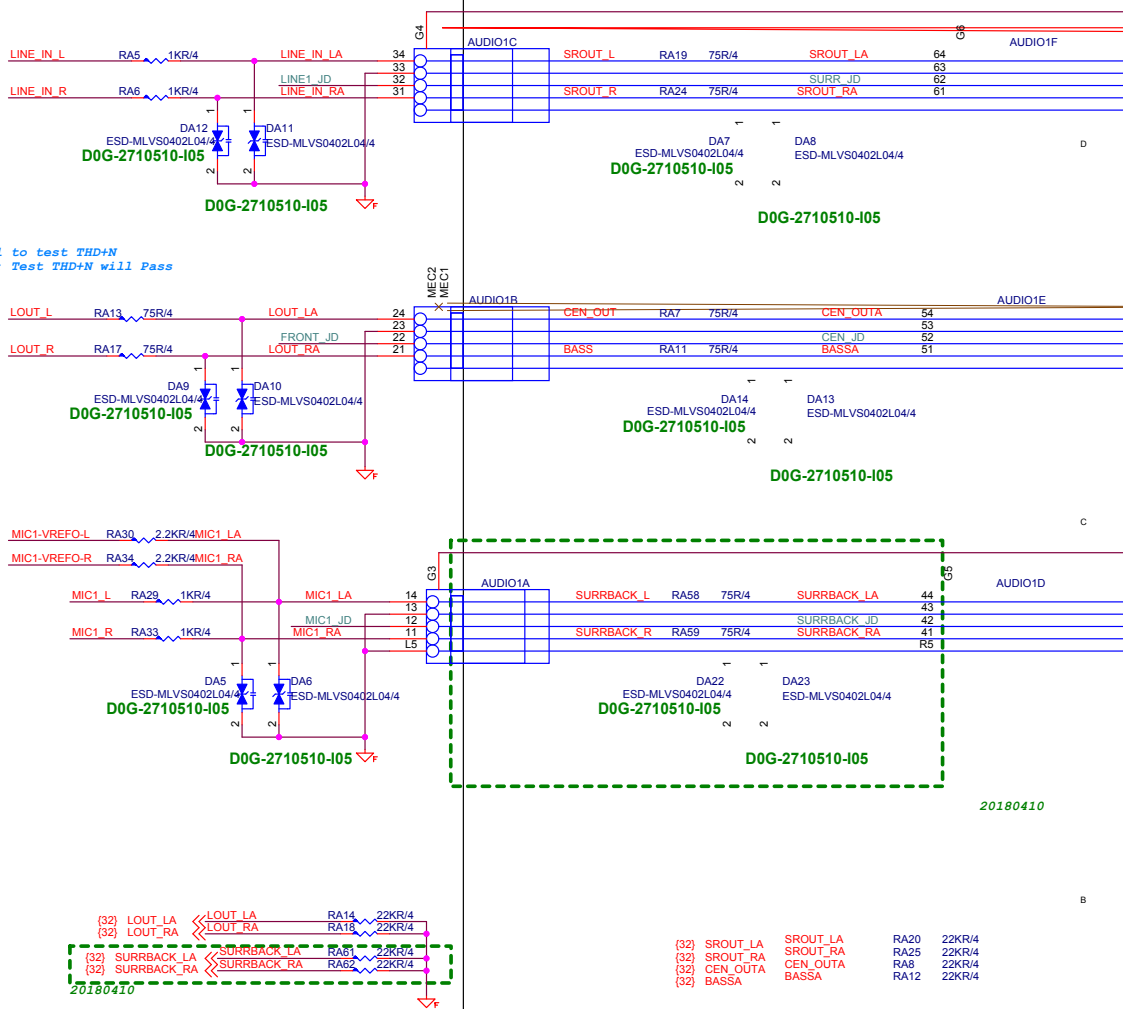
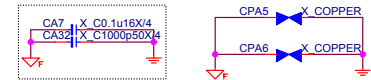
MICRO-STAR INT'L CO.,LTD.		Title	LAN 8111H
		Size	Document Number
Date: Tuesday, December 18, 2018		MS-7C02..	Rev 20
Sheet 30 of 70			

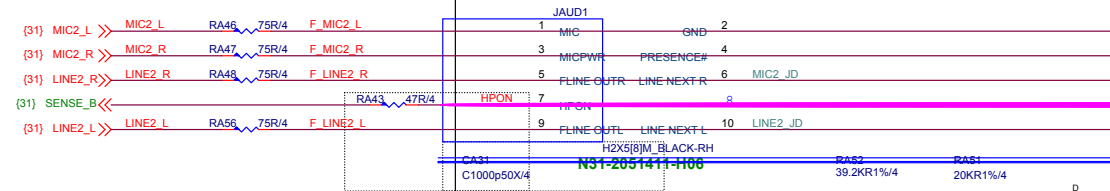
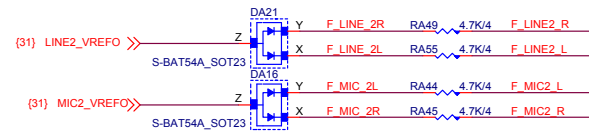
ALC892

Follow APU power well



EMI





Close to Front panel
For HDA/AC97 front cable.

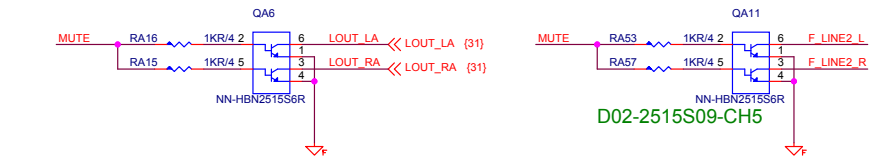
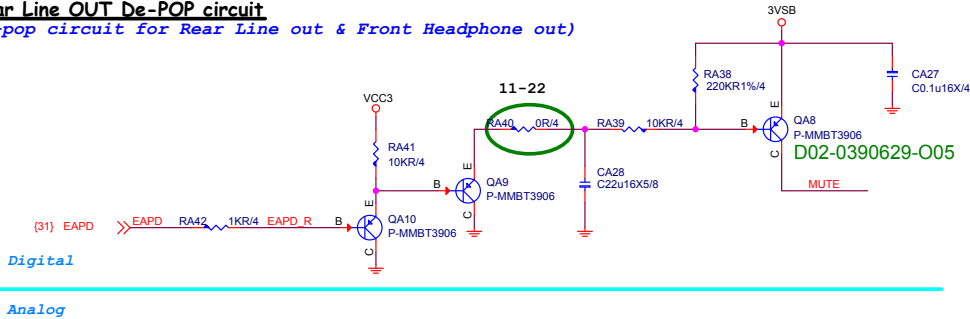
D0G-2710510-I05
Close to Front panel

ESD protect
D0G-2710510-I05
av1:D0G-2950500-SI0

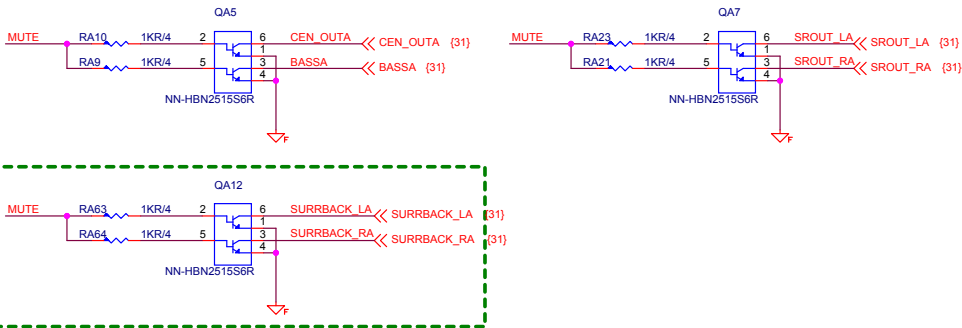
F_LINE2_L RA54 22KR/4
F_LINE2_R RA50 22KR/4

Rear Line OUT De-POP circuit

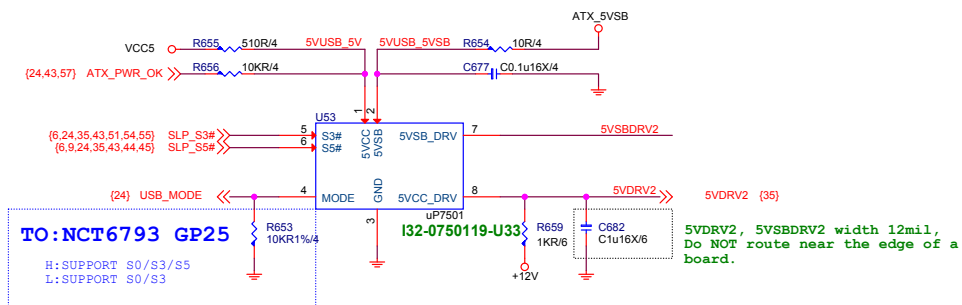
(De-pop circuit for Rear Line out & Front Headphone out)



(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA5,CA6, CA7, CA9,to TVS)

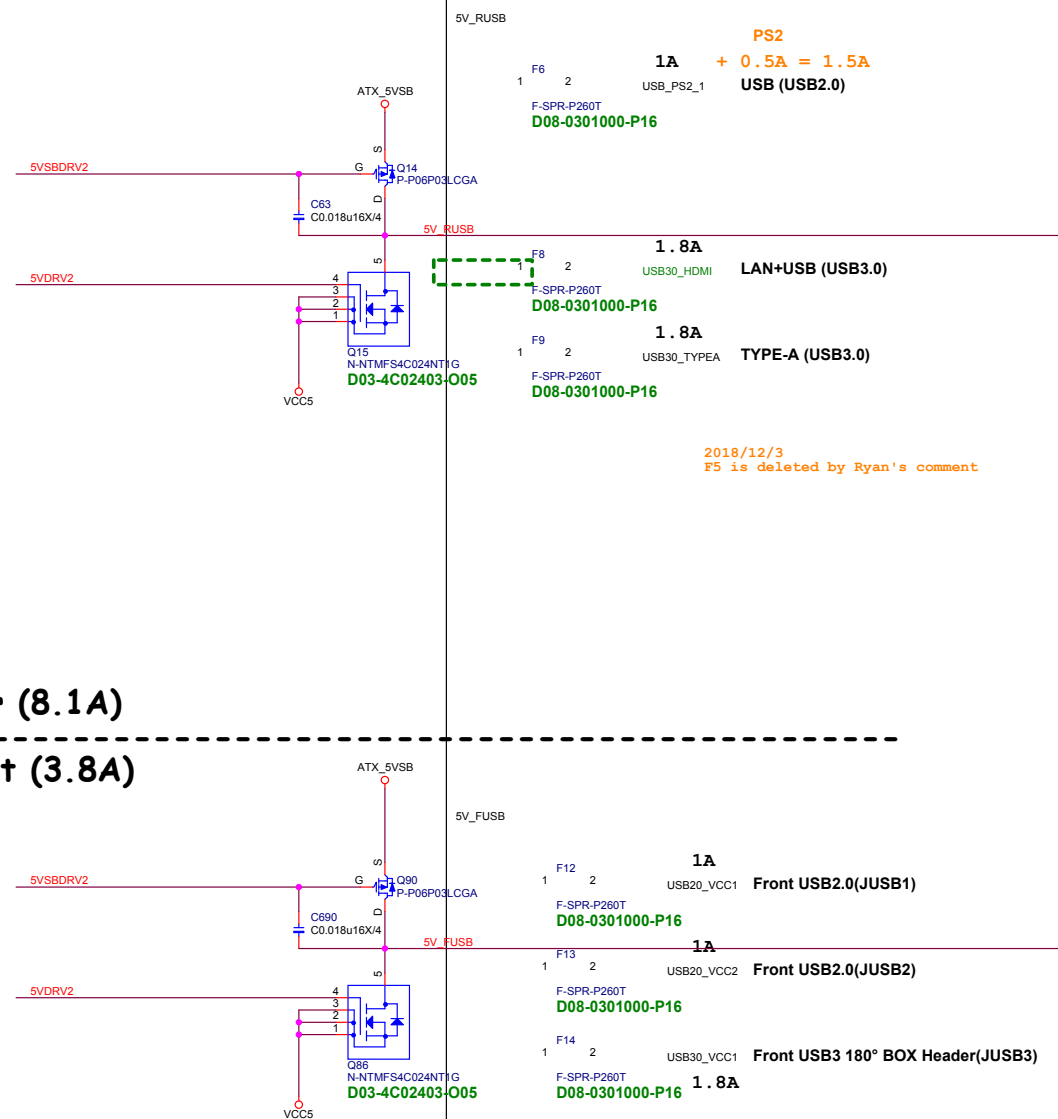


USB Power



Rear (8.1A)

Front (3.8A)

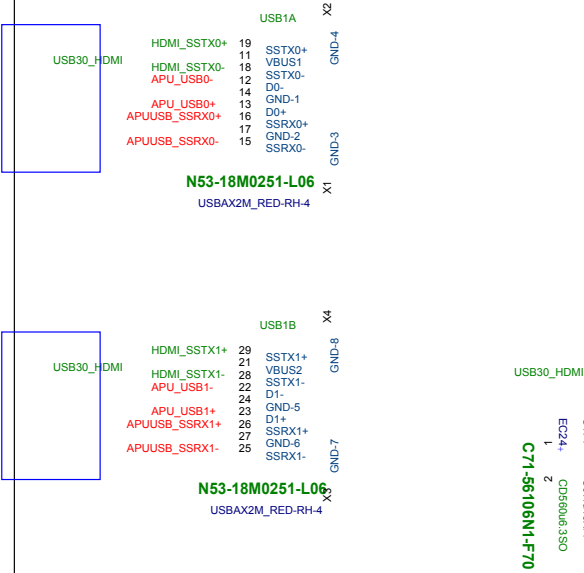
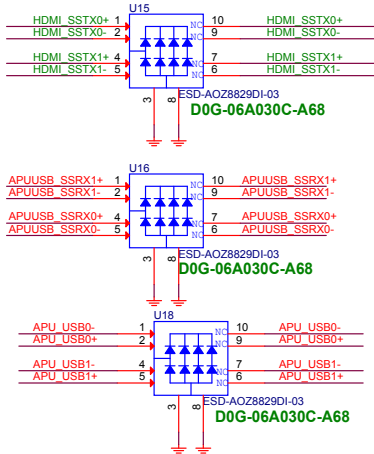
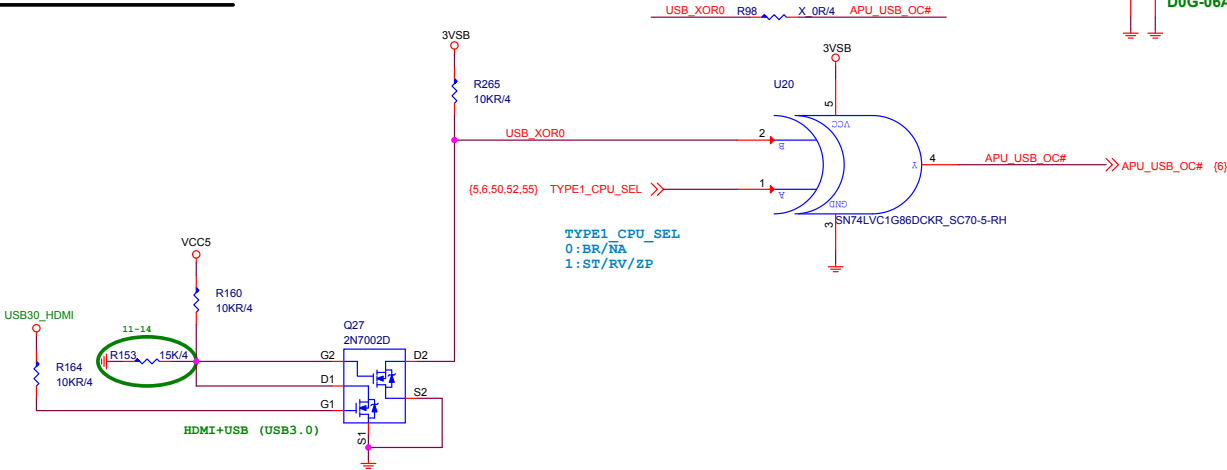


HDMI+USB (USB3.0)

5V@1A

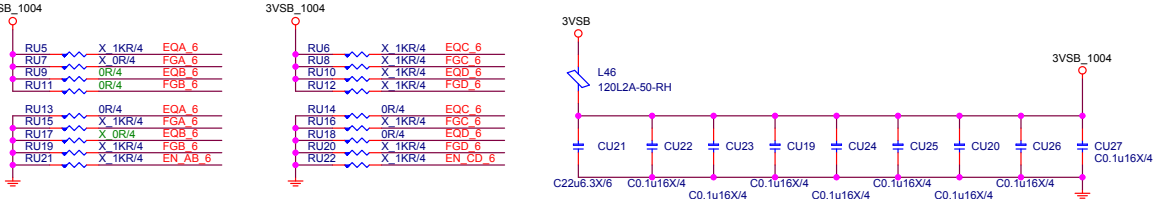
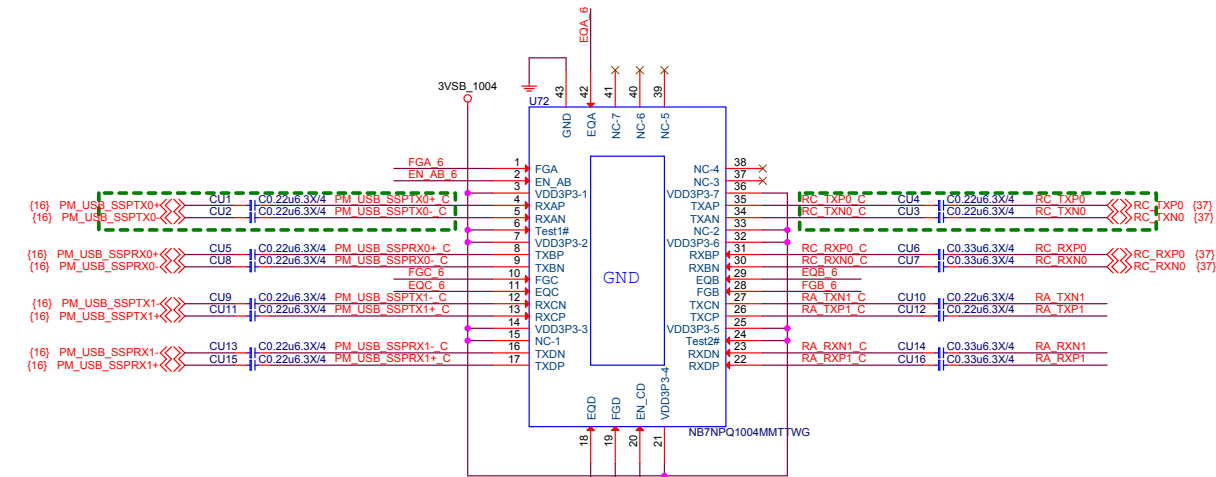
- (7) APU_USB_SSTX0+ <<> C158 C0.22u6.3X/4 HDMI_SSTX0+
- (7) APU_USB_SSTX0- <<> C162 C0.22u6.3X/4 HDMI_SSTX0-
- (7) APU_USB_SSRX0+ <<> C182 C0.33u6.3X/4 APUUSB_SSRX0+
- (7) APU_USB_SSRX0- <<> C187 C0.33u6.3X/4 APUUSB_SSRX0-
- (7) APU_USB_SSTX1+ <<> C163 C0.22u6.3X/4 HDMI_SSTX1+
- (7) APU_USB_SSTX1- <<> C172 C0.22u6.3X/4 HDMI_SSTX1-
- (7) APU_USB_SSRX1+ <<> C176 C0.33u6.3X/4 APUUSB_SSRX1+
- (7) APU_USB_SSRX1- <<> C178 C0.33u6.3X/4 APUUSB_SSRX1-
- (7) APU_USB0+ <<> APU_USB0+
- (7) APU_USB0- <<> APU_USB0-
- (7) APU_USB1+ <<> APU_USB1+
- (7) APU_USB1- <<> APU_USB1-

APU_USB_OC



	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

TYPE-A PI3EQX1004 Redriver

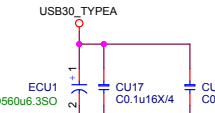


(16) PM_USB0+ >> PM_USB0+
(16) PM_USB0- >> PM_USB0-

RC_TXP0 RU30 200KR1%4
RC_TXN0 RU31 200KR1%4

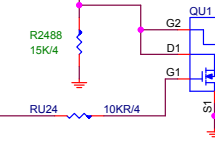
RC_RXP0 RU1 200KR1%4
RC_RXN0 RU2 200KR1%4

RA_RXP1 RU3 200KR1%4
RA_RXN1 RU4 200KR1%4



close to Type C Connector

VCC5
RU23 10KR/4
R2488 15K/4



DU1
ESD-AOZ8829DI-03
1 NC 10
2 NC 9
4 NC 7
5 NC 6
PM_USB0- PM_USB0+ DOG-06A030C-A68

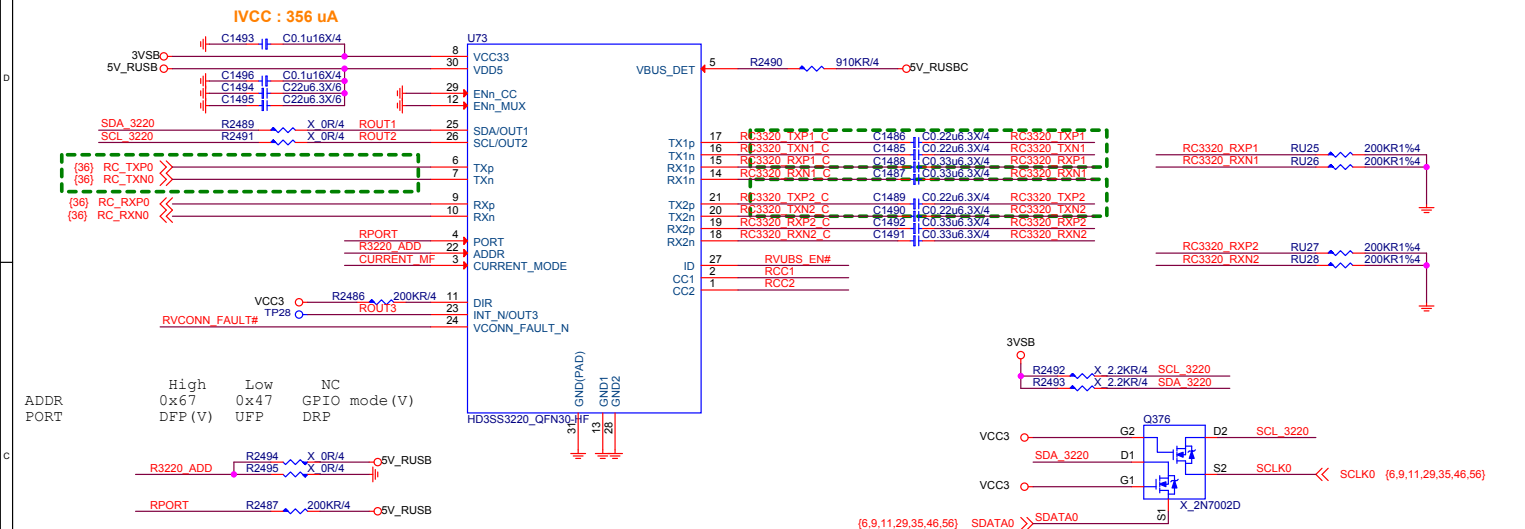
DU2
ESD-AOZ8829DI-03
1 NC 10
2 NC 9
4 NC 7
5 NC 6
RA_TXP1 RA_TXN1 DOG-06A030C-A68
RA_RXP1 RA_RXN1

LAN_USB1A
PM_USB0+ 12
PM_USB0- 11
RA_TXP1 18
RA_TXN1 17
RA_RXP1 15
RA_RXN1 14
SSRX+
SSRX-
RJ45_USB_LEDX2-RH-6
N58-23F0091-F02

EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD

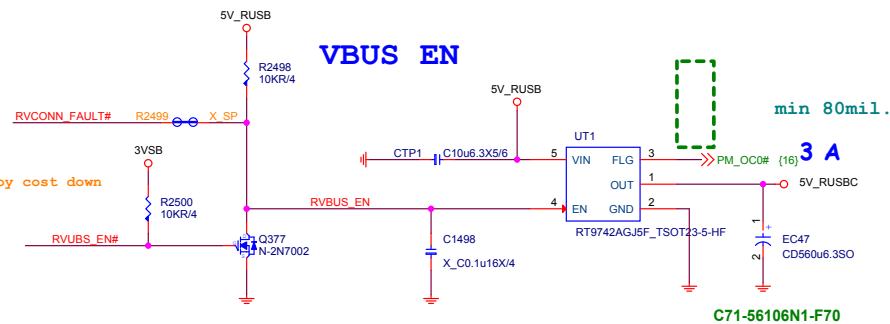
USB 3.1-Type-C USB Type-C MUX with Configuration Channel (CC)



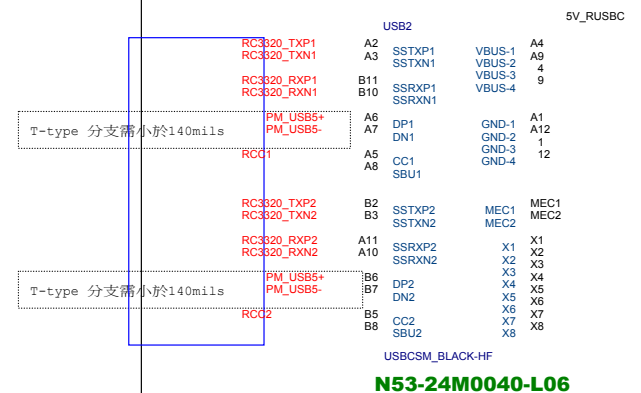
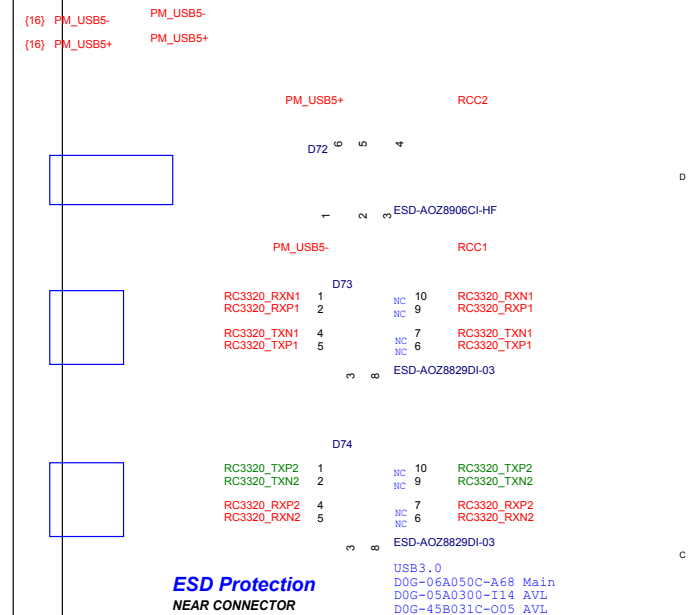
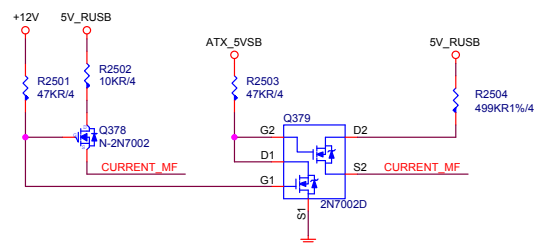
VBUS OC# LEVEL SHIFT



VCOM OC#



Current Mode

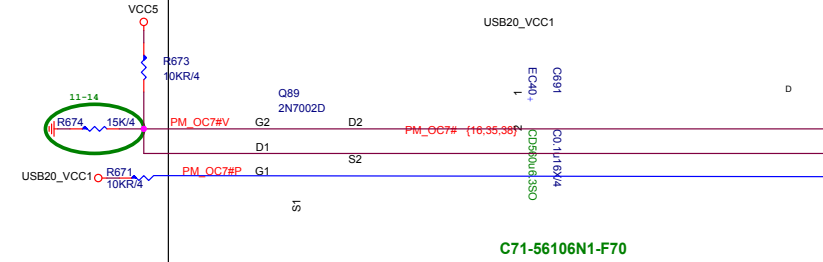
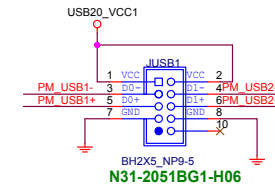
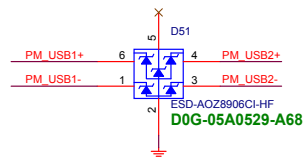
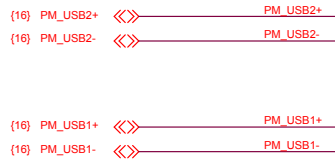


close to Type C Connector

5V_RUSBC	5V_RUSBC
CU28	CU29
C1u6.3X/4	C0.1u16X/4

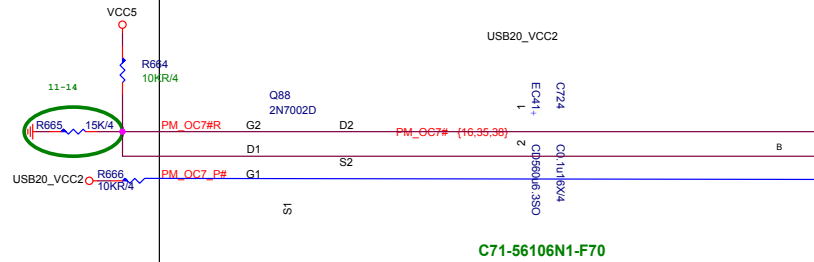
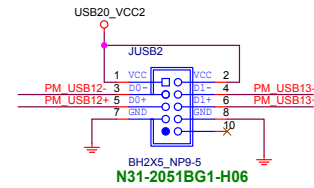
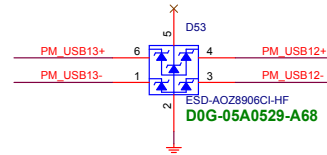
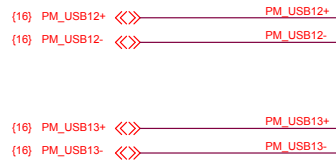
Front USB2.0 (JUSB1)

5V@1A

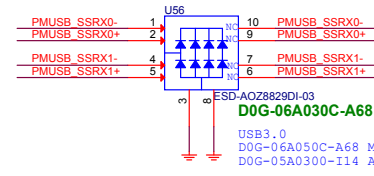
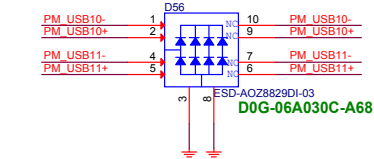
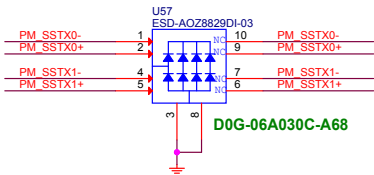
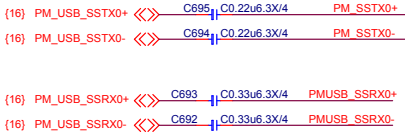


Front USB2.0 (JUSB2)

5V@1A

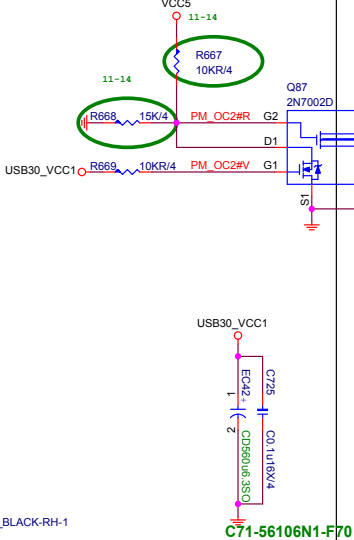
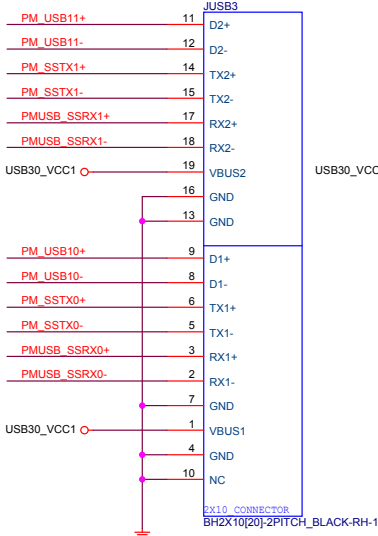


Front USB3 180° BOX Header(JUSB4)
5V@1.8A



USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL



MICRO-STAR INT'L CO.,LTD.

Title Front USB3.0 180° Header

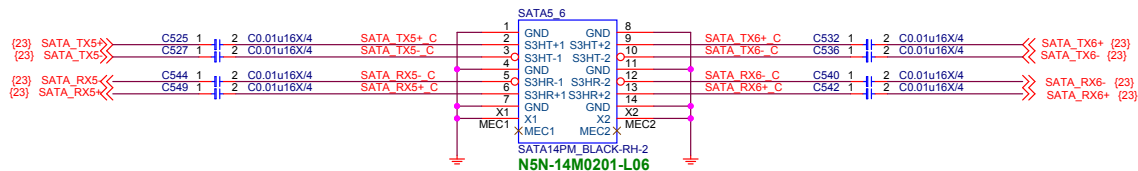
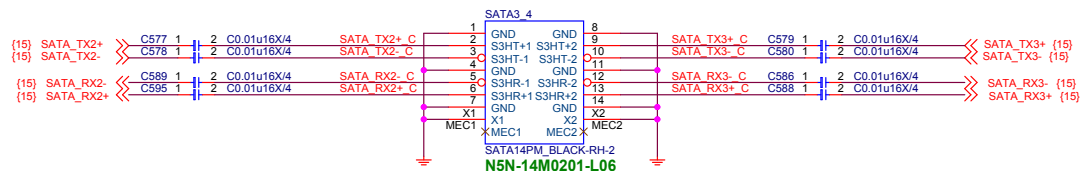
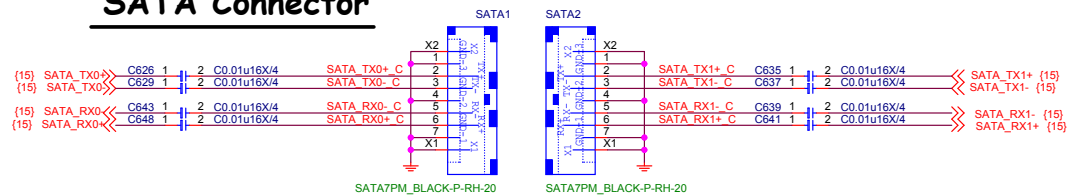
Size Document Number
MS-7C02..

Date: Tuesday, December 18, 2018

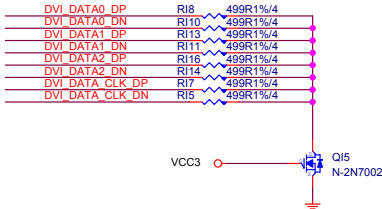
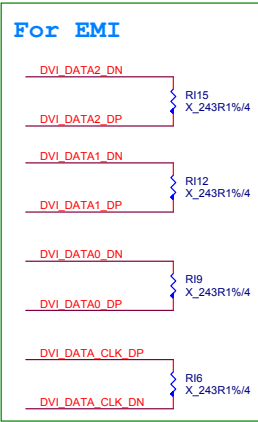
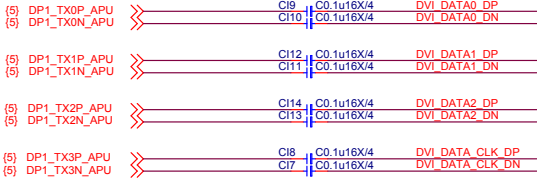
Rev
20

Sheet 39 of 70

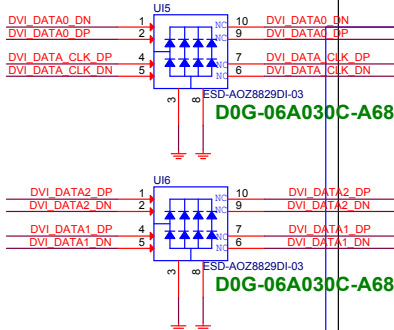
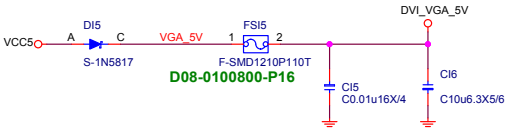
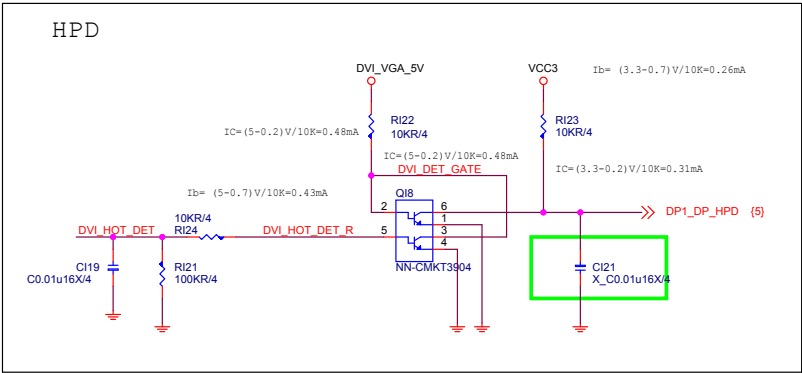
SATA Connector



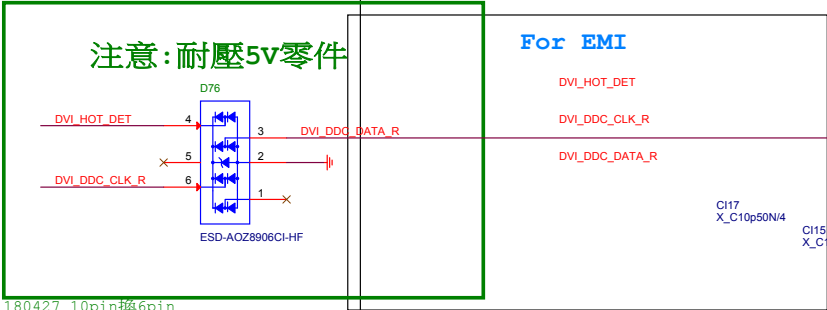
DVI CONNECTOR



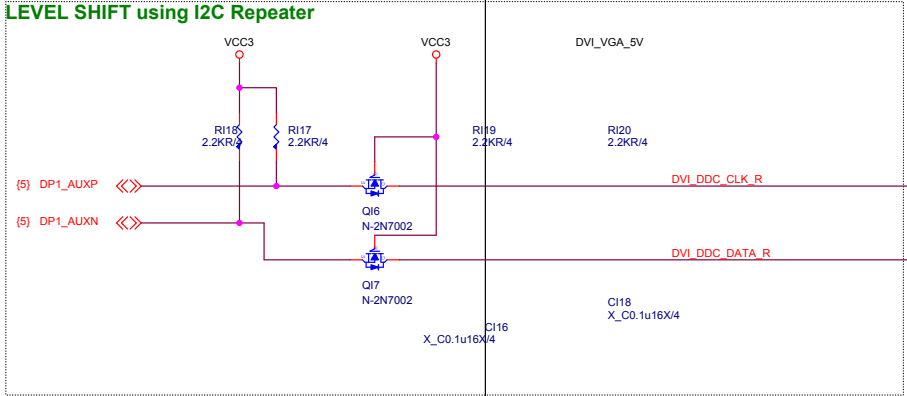
HPD



For EMI



LEVEL SHIFT using I2C Repeater



MICRO-STAR INT'L CO.,LTD.

Title DVI

Size Document Number MS-7C02..

Date: Tuesday, December 18, 2018

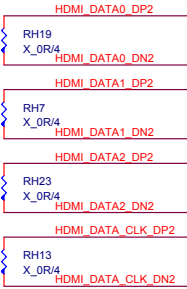
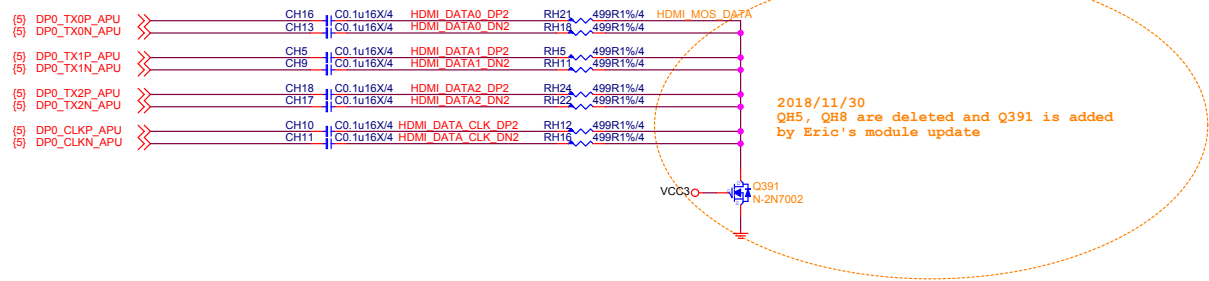
Rev 20

Sheet 41 of 70

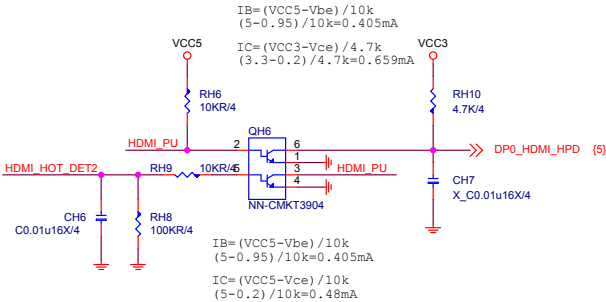
HDMI CONNECTOR

For HDMI 1.4

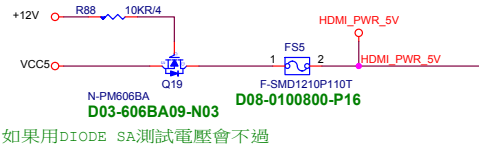
HDMI_MOS_DATA trace length < 500mil
Other platform please check your design guide length



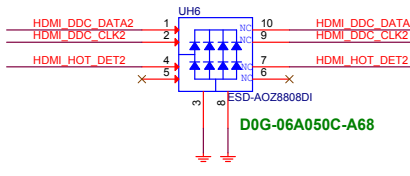
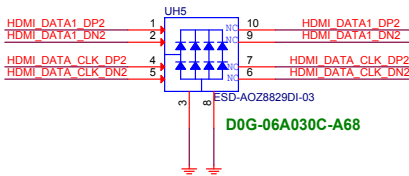
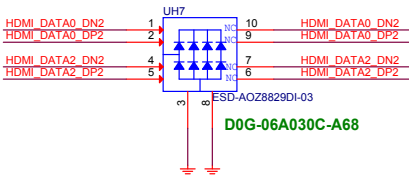
HPD Circuit



Connector Power

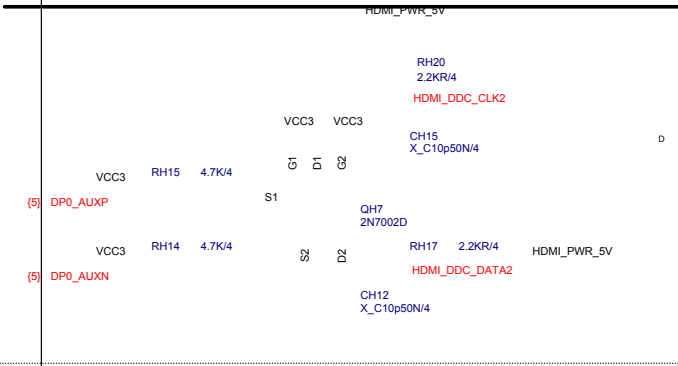


For EMI

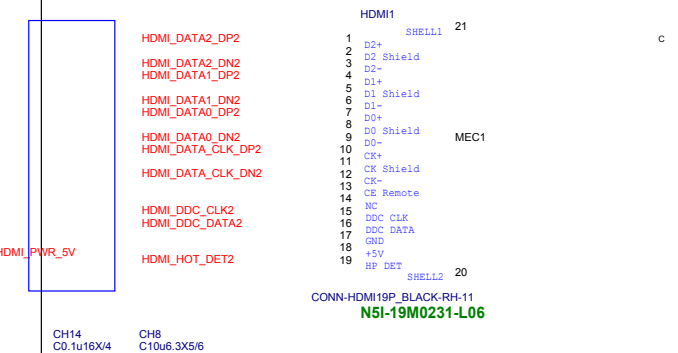


注意: 耐壓5V零件

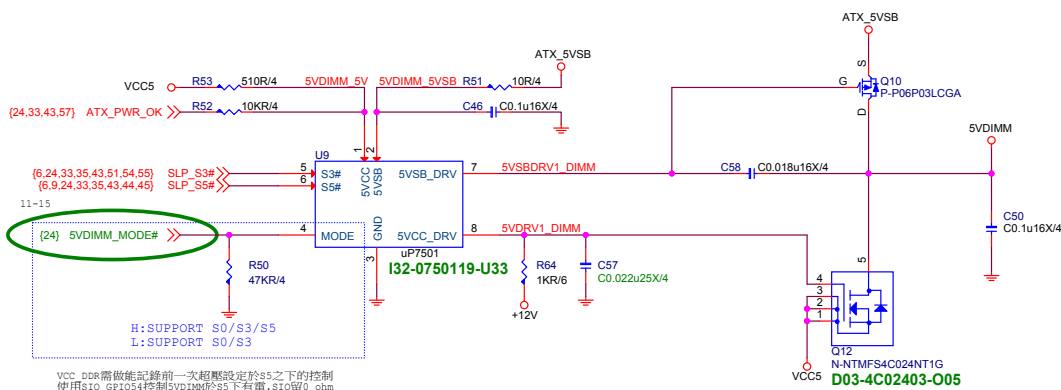
AUX Level Shifter



Connector



5VDIMM FOR DDR



3VSB cost down

3.3V@2.63A

1.05V@0.05A

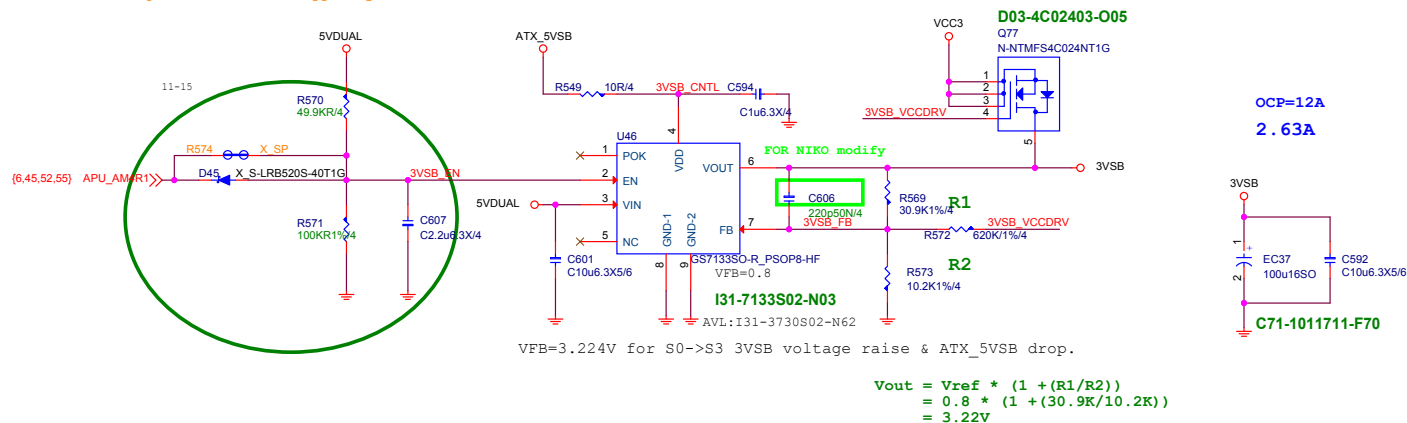
VDDBT_RTC_G@4.5uA

FCH@0.07A

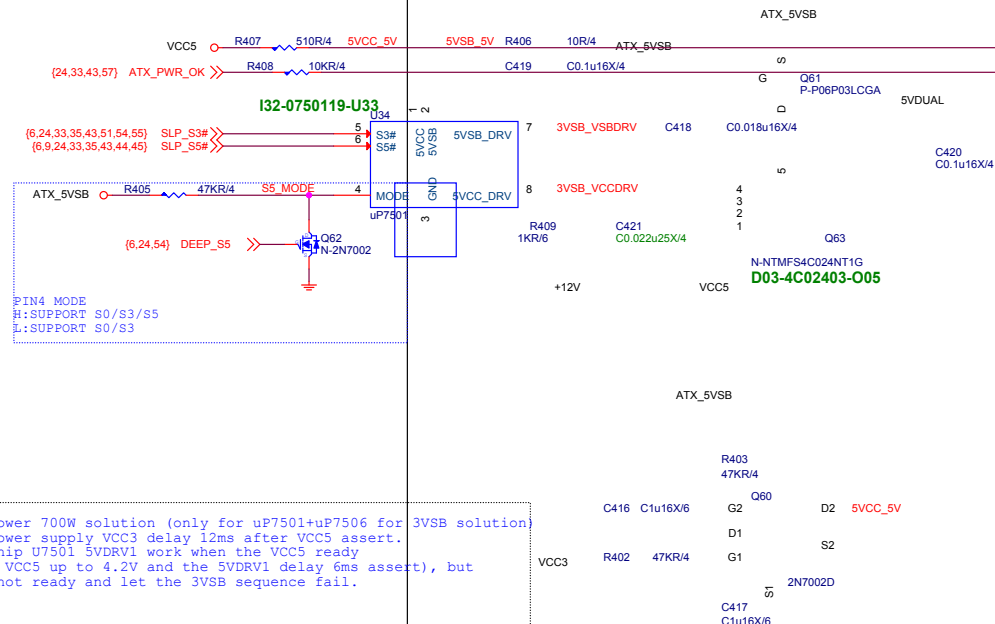
CPU@0.25A

PCIE*6 @2.25A

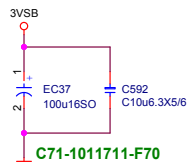
2018/11/26
R574 is changed from 0ohm to copper by cost down



5VDUAL For 3VSB、CPU 1.8V、VDDP

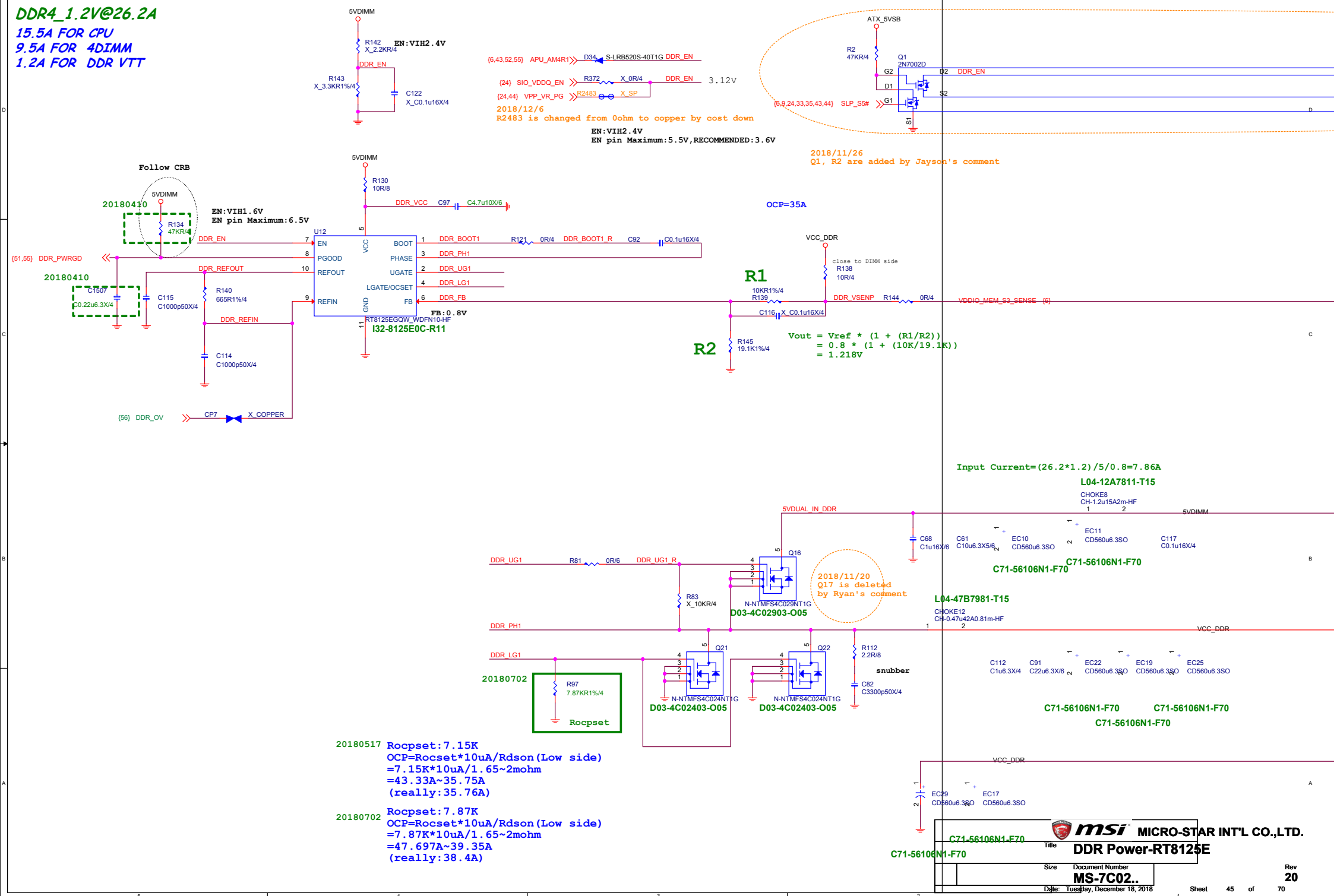


OCP=12A
2.63A



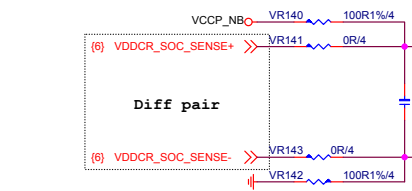
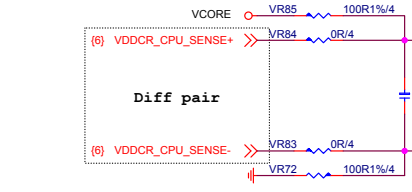
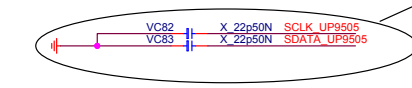
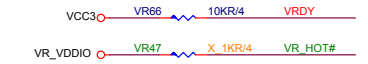
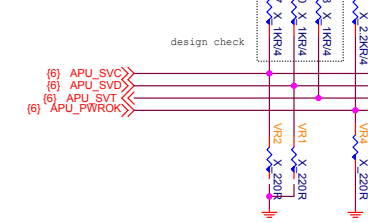
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		Title		ACPI 5VDDIMM/3VSB			
	Size	Document Number				Rev	
		MS-7C02..				20	
Date:		Tuesday, December 18, 2018		Sheet		43	of 70

15.5A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT

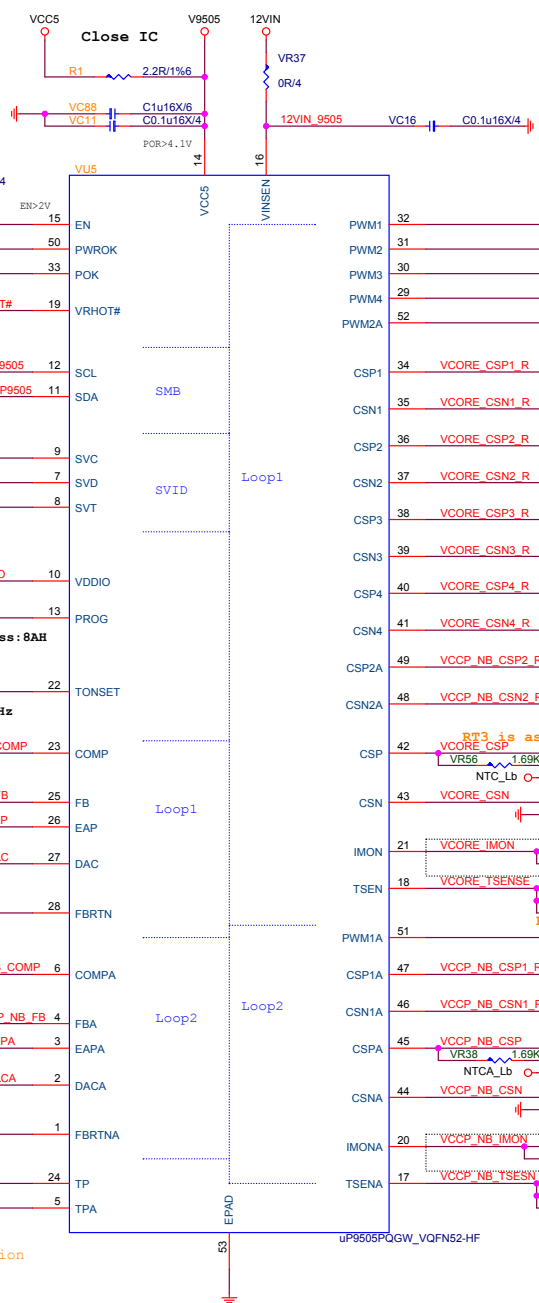


Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

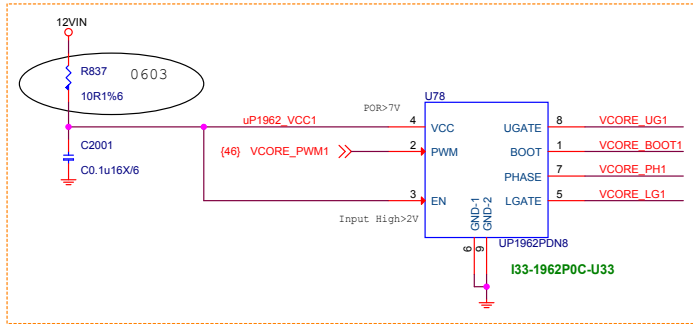


2018/11/22
VR153, VR154 are reserved by UPI's suggestion

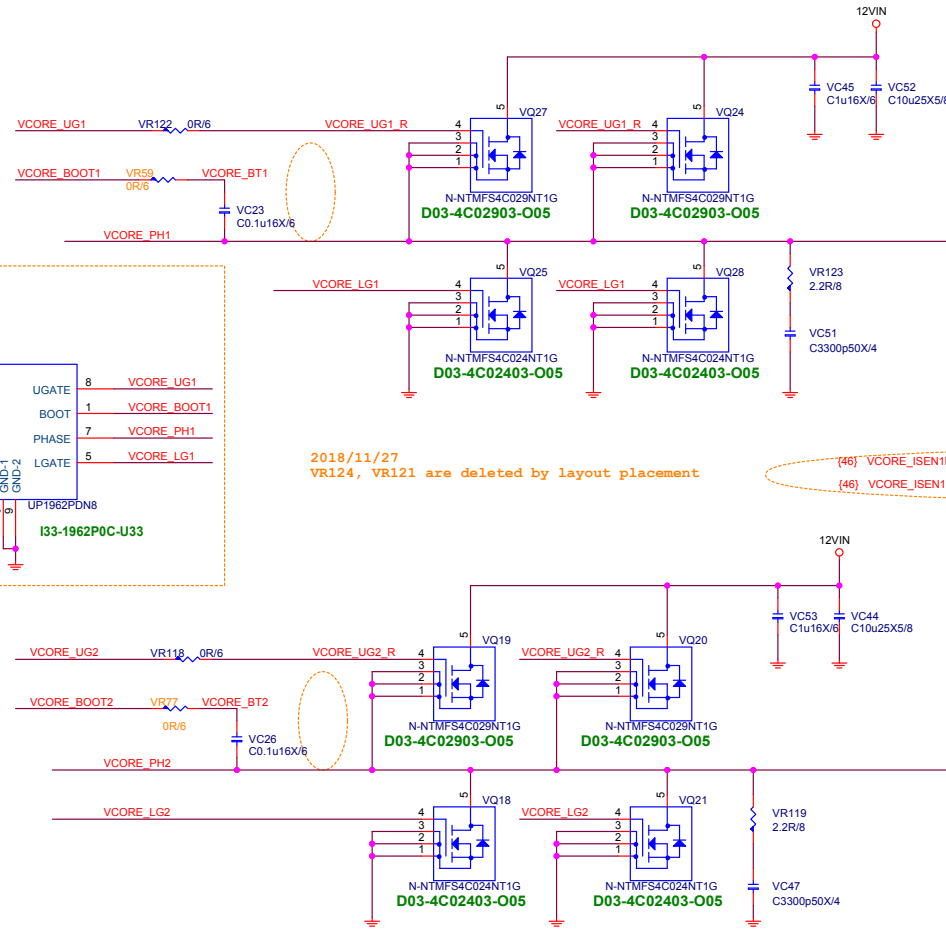


VCORE: ICCMax 140A SET1 control ICCMAX, OCP setting
LL: 1.3mohm SET2 control Internal compensation
OCP: 200A

SOC: ICCMax 75A
LL: 2.1ohm
OCP: 90A



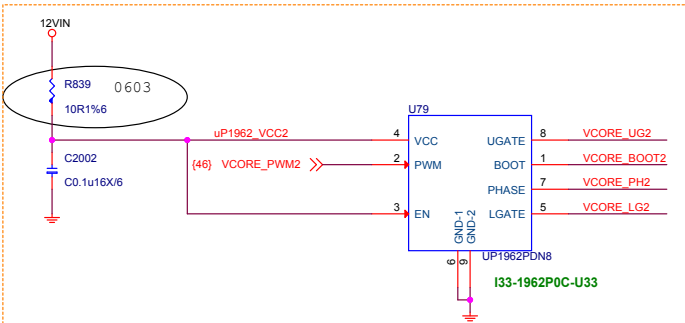
2018/11/27
VR124, VR121 are deleted by layout placement



CH0KE14
CH-0.22u48A0.54m-HF
L04-22B7601-T15

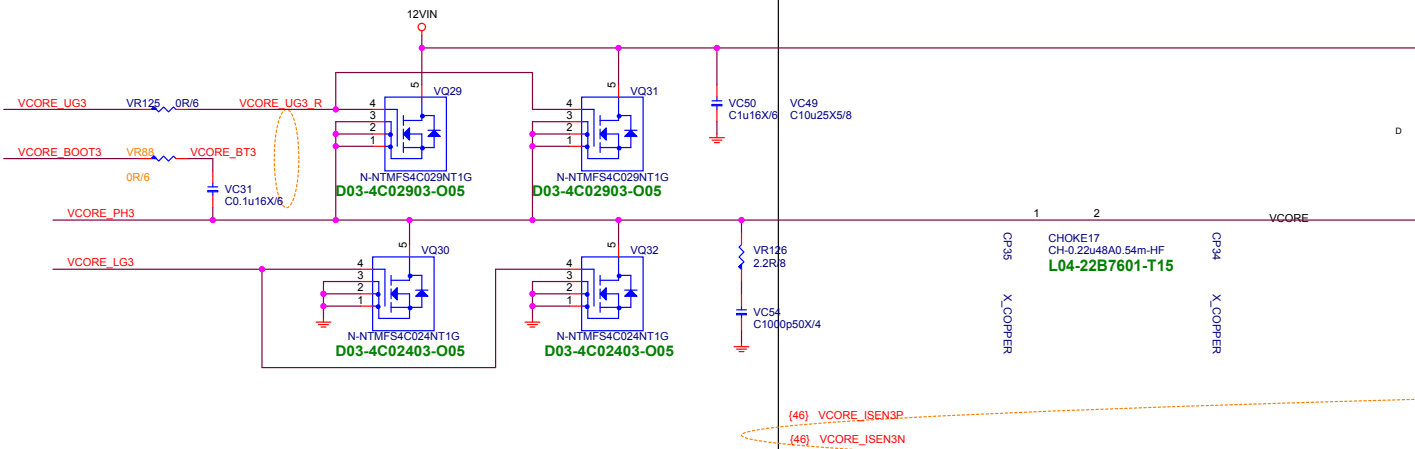
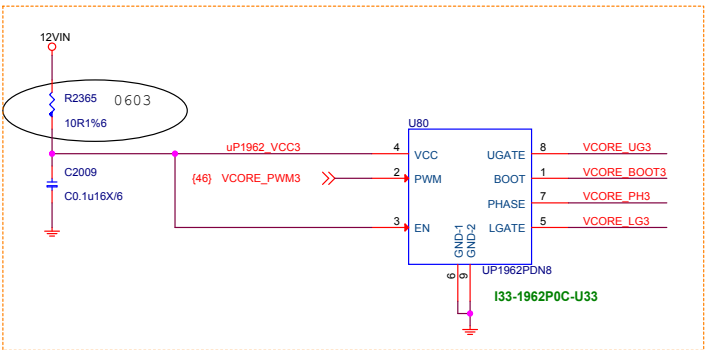
20180412

EC28 1+ 2 CD560u6.3SO
EC13 1+ 2 CD560u6.3SO
EC16 1+ 2 CD560u6.3SO
EC18 1+ 2 CD560u6.3SO
EC21 1+ 2 CD560u6.3SO
EC23 1+ 2 CD560u6.3SO
EC26 1+ 2 CD560u6.3SO
C71-56106N1-F70

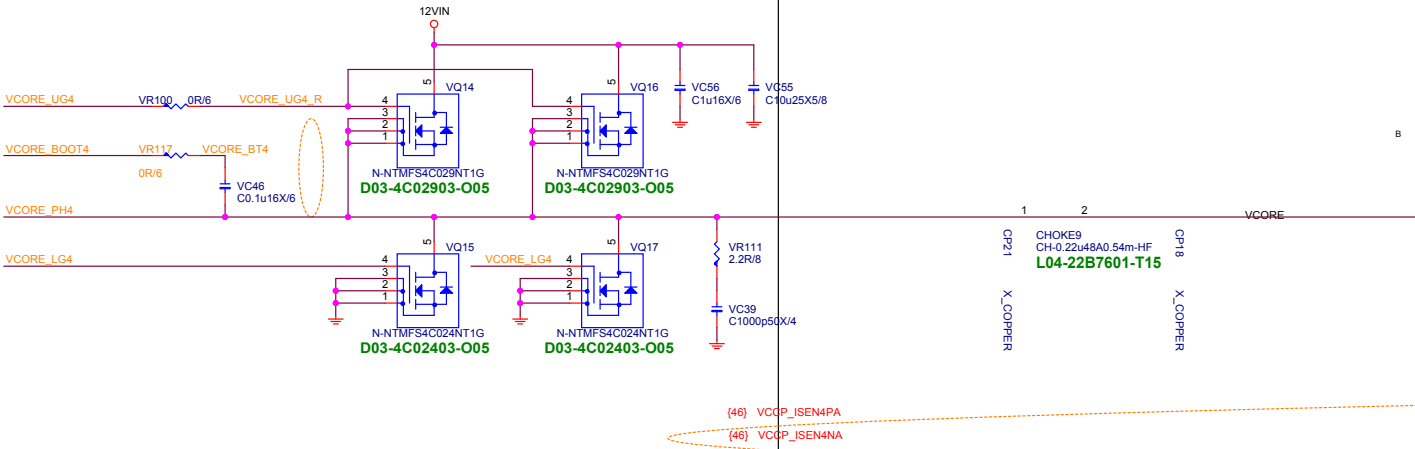
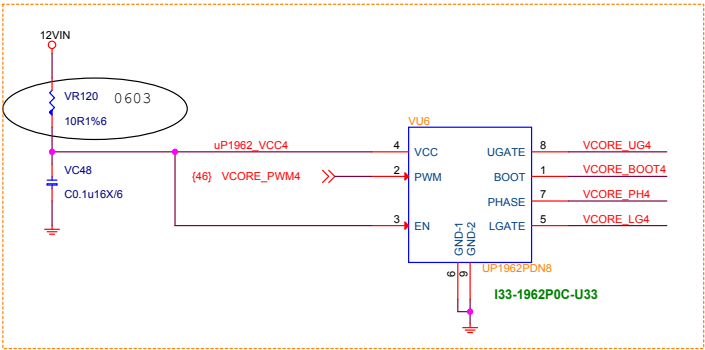


(46) VCORE_ISEN2P <<
(46) VCORE_ISEN2N >>

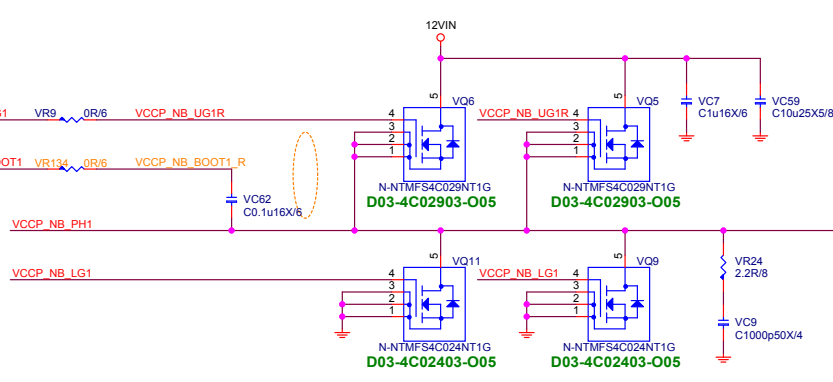
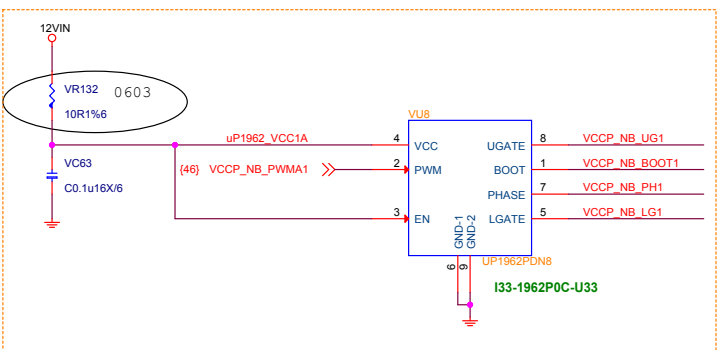
CH0KE11
CH-0.22u48A0.54m-HF
L04-22B7601-T15



2018/11/27
VR127, VR116 are deleted by layout placement



(46) VCCP_ISEN4PA
(46) VCCP_ISEN4NA



L04-22B7601-T15
CHOKE7
CH-0.22u48A0.54m-HF

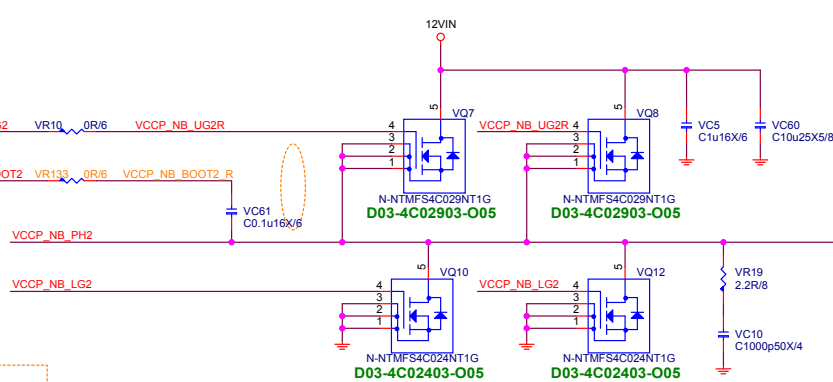
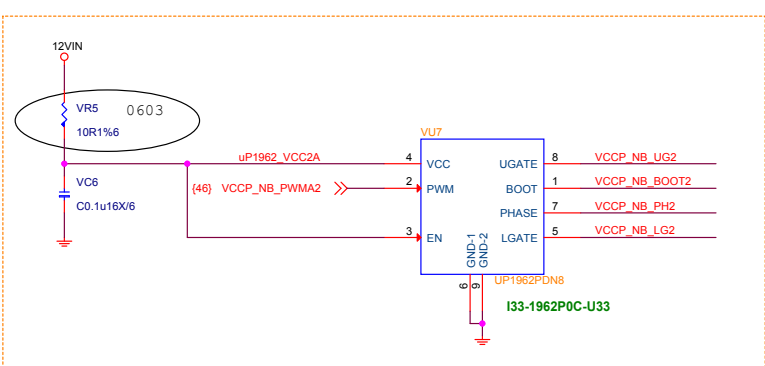
Cp13 X_COOPER
Cp17 X_COOPER

2018/11/27
VR6, VR7 are deleted by layout placement

(46) VCCP_NB_ISEN1PA
(46) VCCP_NB_ISEN1NA

Under checking

VCCP_NB
C71-56106N1-F70
EC7 1+ 2 CD560u6.3SO
EC8 1+ 2 CD560u6.3SO
EC6 1+ 2 CD560u6.3SO
EC43 1+ 2 CD560u6.3SO



L04-22B7601-T15
CHOKE8
CH-0.22u48A0.54m-HF

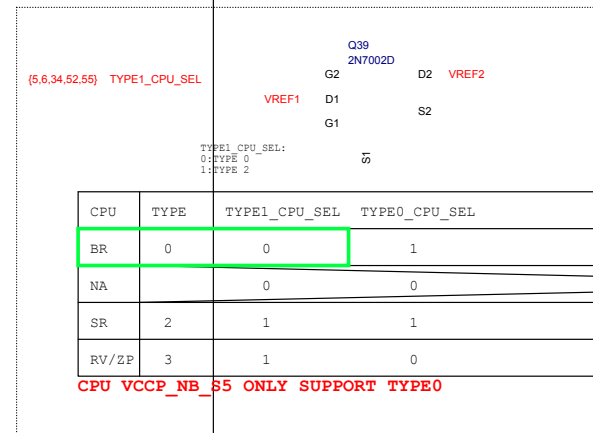
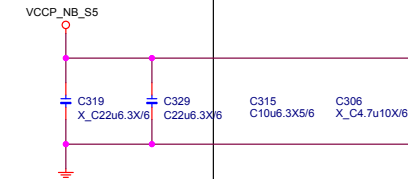
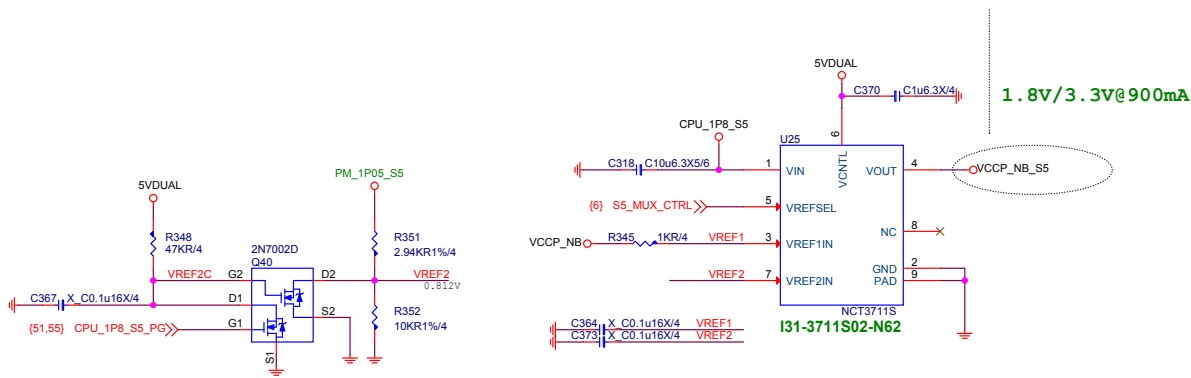
Cp12 X_COOPER
Cp16 X_COOPER

(46) VCCP_NB_ISEN2PA
(46) VCCP_NB_ISEN2NA

S5_MUX_CTRL
HIGH: S0
LOW: S3/S5

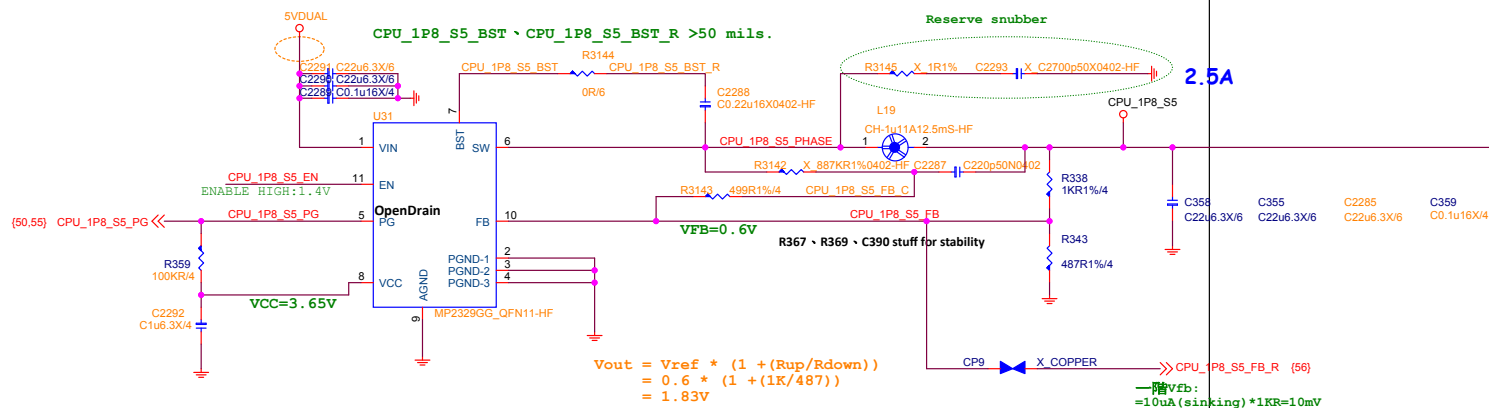
H: +VDDCR_FCH ALW will track VDDNB
L: If $VDD\overline{C}R_SOC < 0.775V$ (OR 0.85V), $VDD\overline{C}R_SOC_S5 = 0.775V$.
If $VDD\overline{C}R_SOC \geq 0.775V$ (OR 0.85V), $VDD\overline{C}R_SOC_S5$ will track $VDD\overline{C}R_NB$

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)

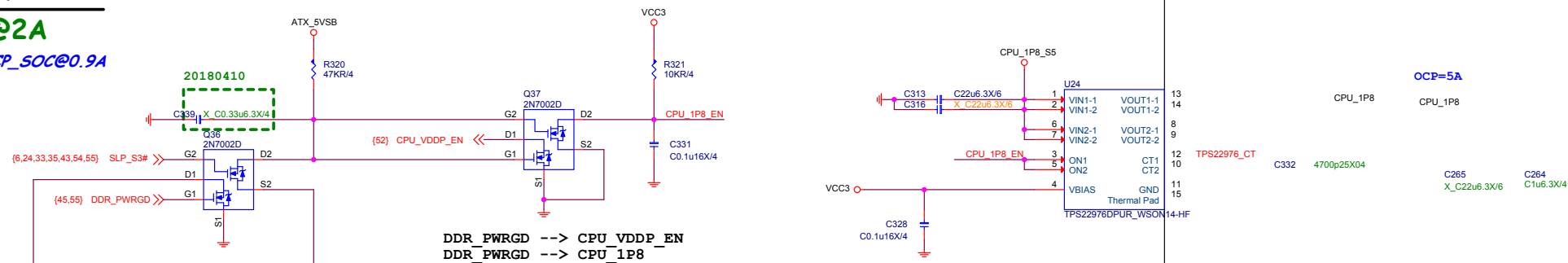


```
1.8V S5@0.5A
1.8V S0@2A
0.9A(VCCP_NB_S5)
```

CPU 1P8 S5 BST、CPU 1P8 S5 BST R >50 mils.



1.8V@2A
FOR VCCP_SOC@0.9A



OCP=5A

Title **CPU 1.8 S0/S5**

Size	Document Number
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CPU_VDDP_S0

1.05V/0.9V@S0:8.5A

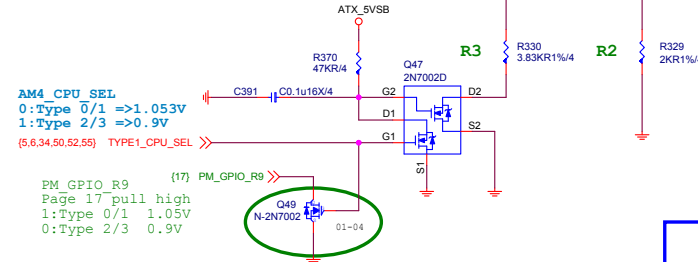
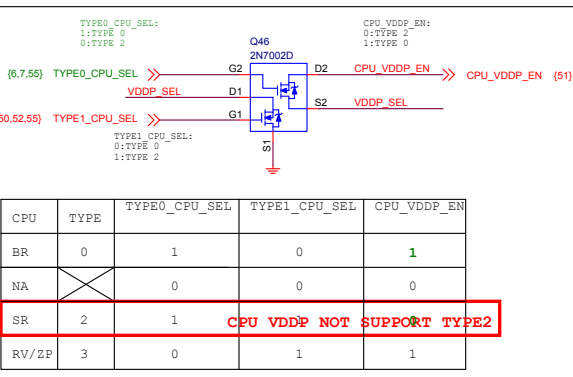
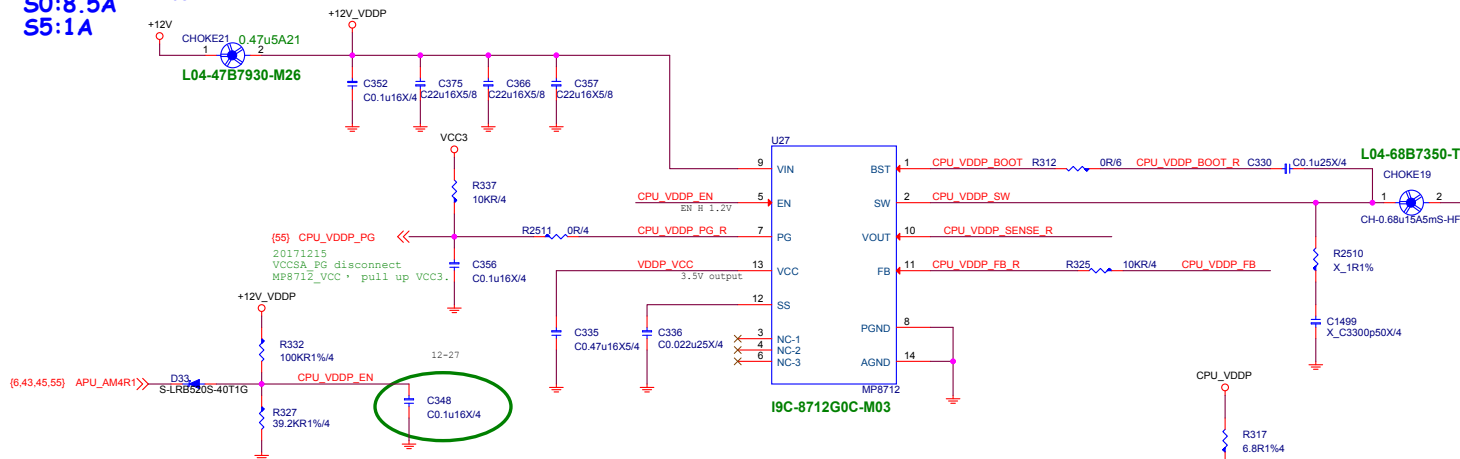
S0:8.5A
S5:1A

Input Current= (8.5A*1.05V)/12V/0.8=0.93A

OCP=14A

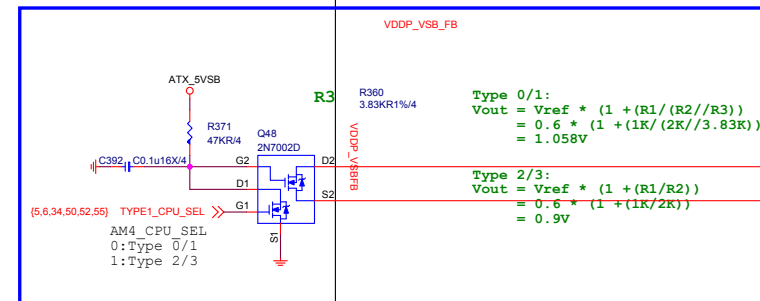
1.05V,8.5A

CPU_VDDP



Type 0/1:
 $V_{out} = V_{ref} * (1 + (R1/(R2//R3)))$
 $= 0.6 * (1 + (1K/(2K//3.83K)))$
 $= 1.056V$

Type 2/3:
 $V_{out} = V_{ref} * (1 + (R1/R2))$
 $= 0.6 * (1 + (1K/2K))$
 $= 0.9V$



Type 0/1:
 $V_{out} = V_{ref} * (1 + (R1/(R2//R3)))$
 $= 0.6 * (1 + (1K/(2K//3.83K)))$
 $= 1.058V$

Type 2/3:
 $V_{out} = V_{ref} * (1 + (R1/R2))$
 $= 0.6 * (1 + (1K/2K))$
 $= 0.9V$

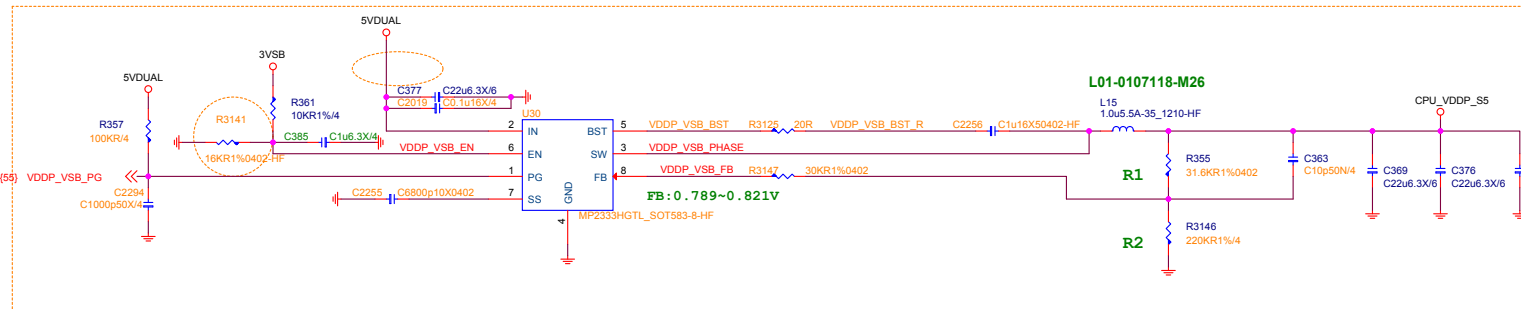
CPU_VDDP_S5

1.05V/0.9V
S5:1A

2018/12/5
U30 is changed from MP2143 to MP2333H and L18 is deleted by Ryan's comment

2018/12/11

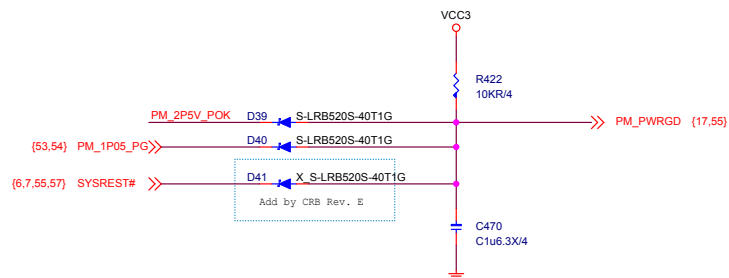
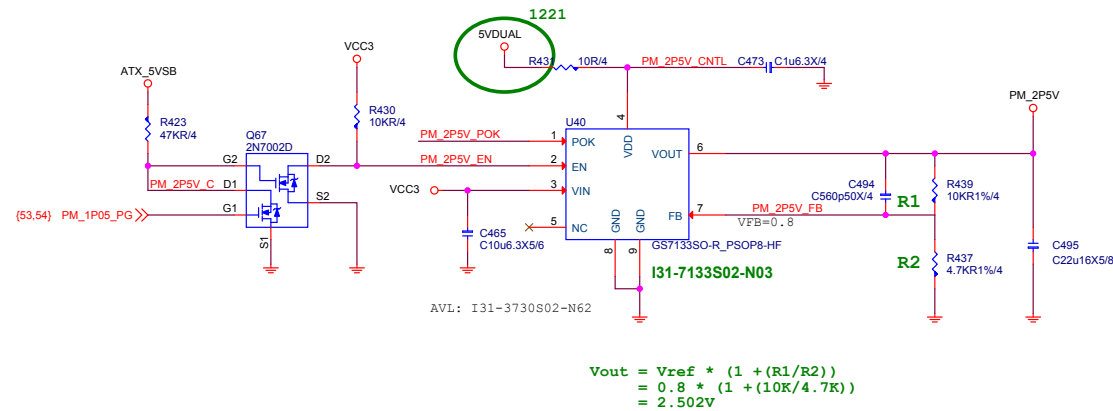
R3141 is changed to 16kohm by Ryan's comment



$V_{out} = V_{ref} * (1 + (R_{up}/R_{down}))$
 $= 0.789 \sim 0.821V * (1 + (31.6K/220K))$
 $= 0.902V \sim 0.938V$

Promontory-2.5V

2.5V@900mA



MICRO-STAR INT'L CO.,LTD.

Title Prom-GS7133/2.5V

Size Document Number
MS-7C02..

Date: Tuesday, December 18, 2018

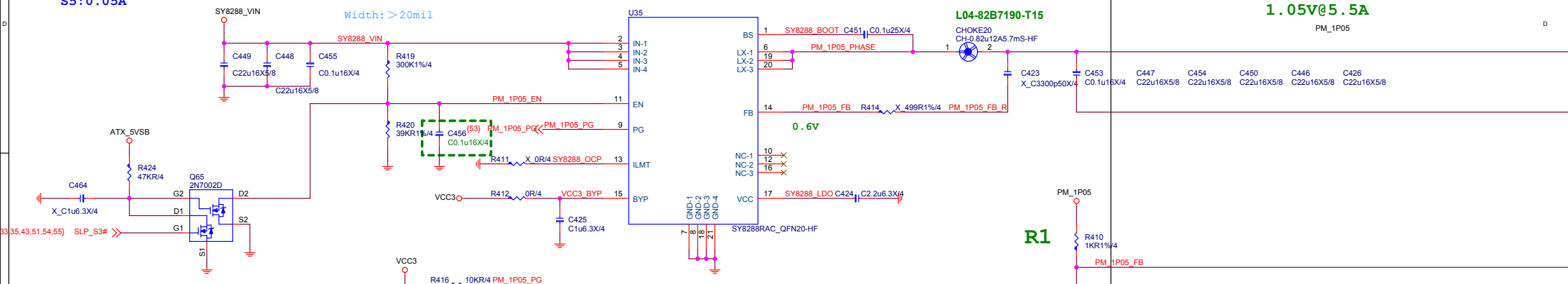
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20

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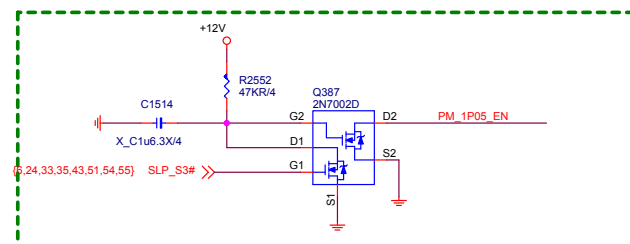
1.05V
S0:5.5A
S5:0.05A

Input Current= (5.5A*1.05V)/12V/0.8=0.6A

OCP=12A
1.05V@5.5A
PM_1P05



SY8288_OCP	OCP
0	8A
floating	12A
1	16A



R1

R410
1KR1%4

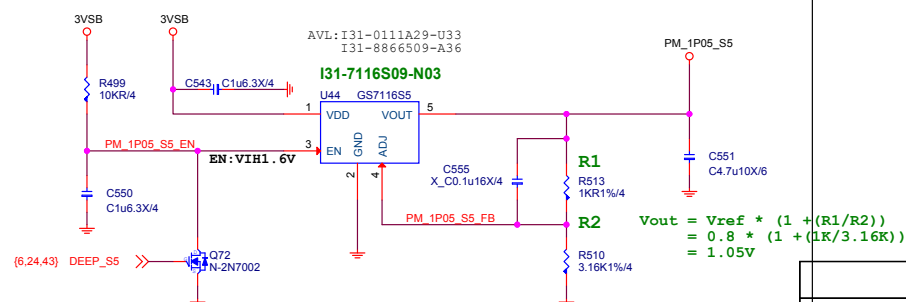
PM_1P05_FB

R2

R413
1.33K1%4

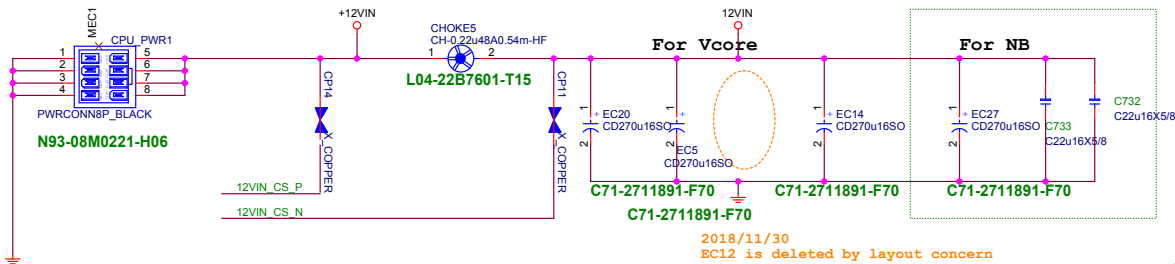
$$V_{out} = V_{ref} * (1 + (R1/R2))$$
$$= 0.6 * (1 + (1K/1.33K))$$
$$= 1.051V$$

1.05V@0.05A

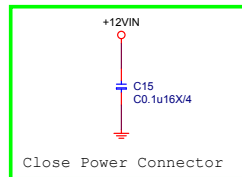


$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R_1/R_2)) \\ &= 0.8 * (1 + (1K/3.16K)) \\ &= 1.05V \end{aligned}$$

CPU POWER CONNECTOR



NB		VCCP	
D=Vout/Vin		D=Vout/Vin	
Vin = 12	> input voltage	Vin = 12	> input voltage
Vout = 1.4	> output Vcore	Vout = 1.4	> output Vcore
D = 0.116667		D = 0.116667	
Io = Icoremax*0.8		Io = Icoremax*0.8	
I core(max) = 75	> Vcore current	I core(max) = 125	> Vcore current
I avg. = 75	A	I avg. = 125	A
I ripple (Io / D * (1-D)) / Phase		I ripple (Io / D * (1-D)) / Phase	
Phase = 12	phase	Phase = 12	phase
I ripple = 12.03835	A	I ripple = 10.03196	A
How many pcs. Of Cap.		How many pcs. Of Cap.	
I ripple(cap) = 5000	m A	I ripple(cap) = 5000	m A
COE _{max} = 1		COE _{max} = 1	
Input Cap. = 3	pcs.	Input Cap. = 3	pcs.

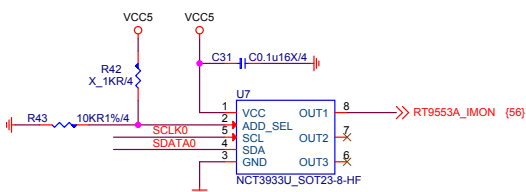


Over Voltage Control IC

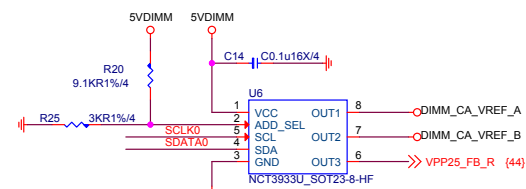
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

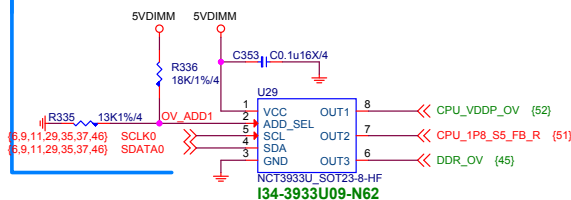
0x2A: RH=OPEN, RL=10K



0x28: RH=9.1K, RL=3K

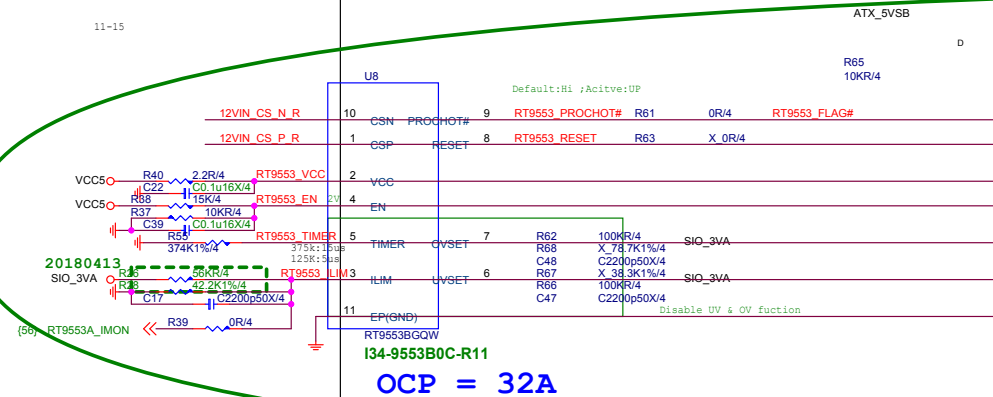


0x26: RH=18K, RL=13K

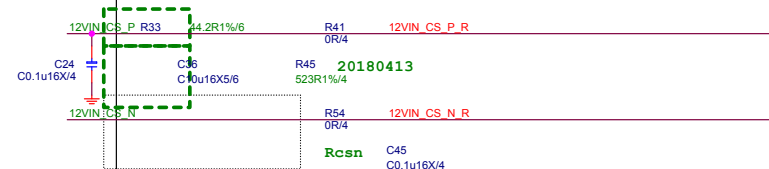


RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.



20180413



RT8894_EN (46.55)

Q11
N-2N7002

2018/11/26
R16 is changed from 0ohm to copper by cost down

ATX_5VSB
R19 47KR/4

RT9553_FLAG# G
RT9553_FLAG# G1

2N7002D

2018/12/12
D5 is unstuffed by Ryan's comment

D5, X S-LR6520S-40T1G APU_THERMTRIP# (6)



MICRO-STAR INT'L CO.,LTD.

Title RT9553B CURRENT SENSE/OV Control

Size Document Number MS-7C02..

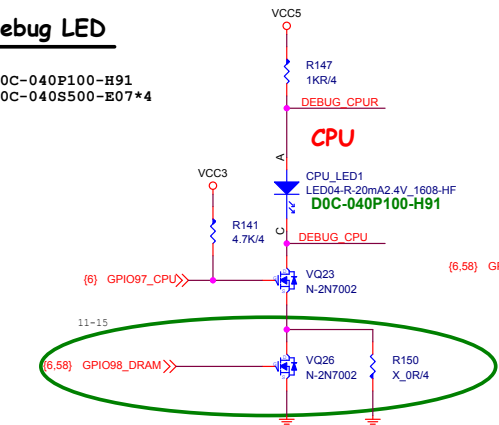
Date: Tuesday, December 18, 2018

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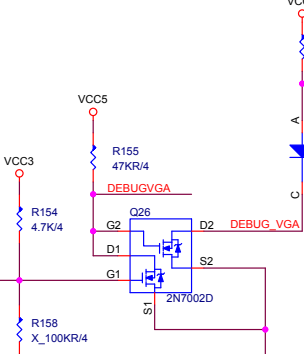
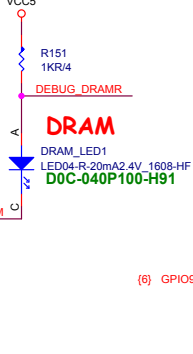
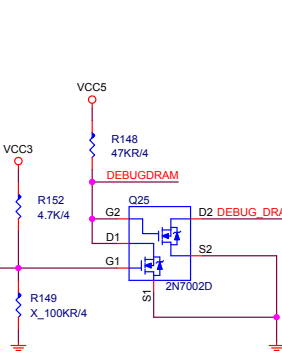
Rev 20

EZ Debug LED

紅:M:D0C-040P100-H91
S:D0C-040S500-E07*4

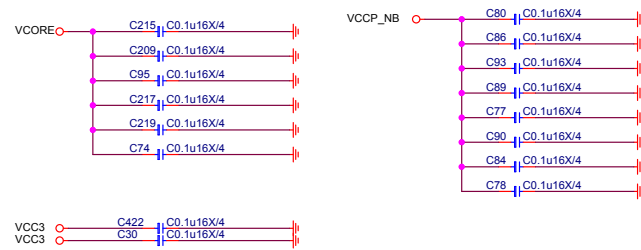


(6.58) GPIO98_DRAM

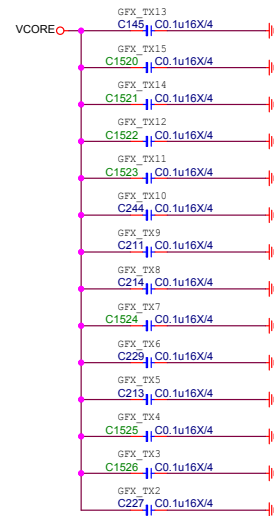
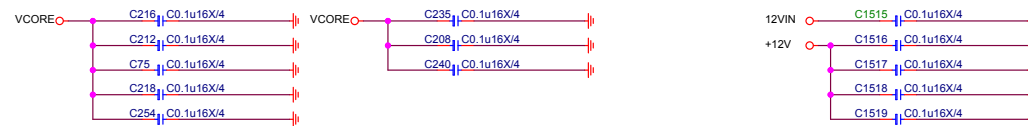


LED	GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮		GPI FULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅		GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

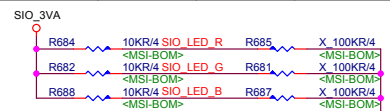
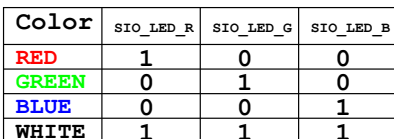
Add for EMI



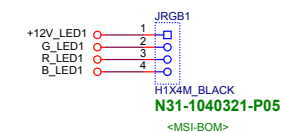
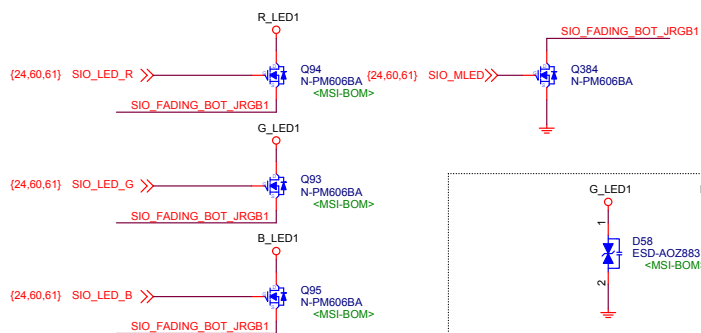
return path



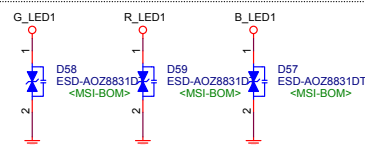
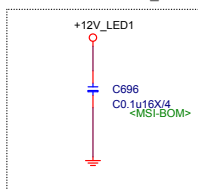
2016.07.06 Use TPS25944L



PM SPEC Default WHITE Color



2016.08.02 Add +12V LED 0.1uF

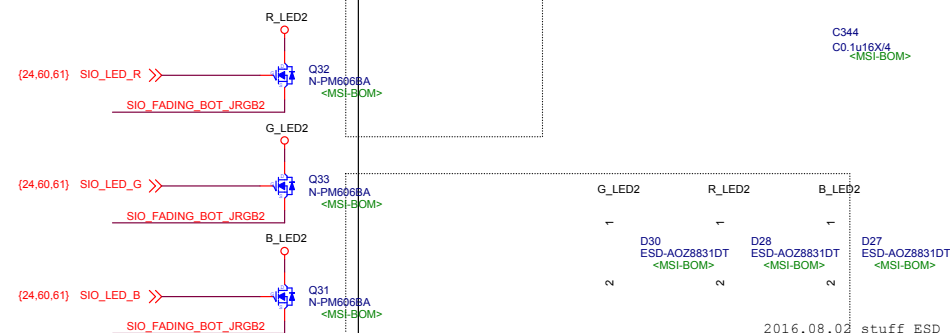


2016.08.02 stuff ESD

2016.07.06 Use TPS25944L

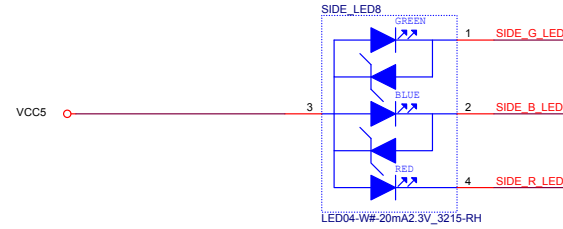
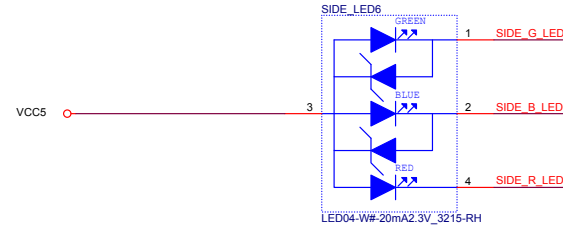
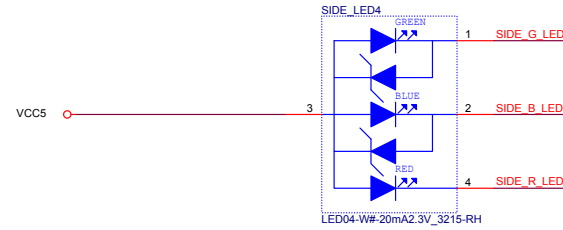
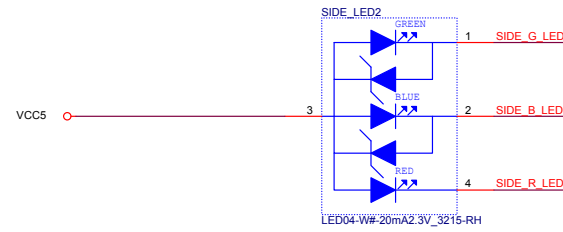
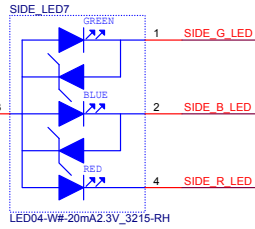
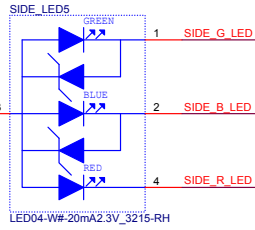
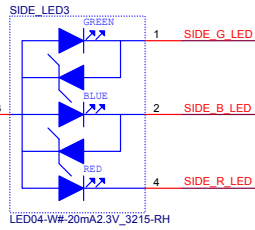
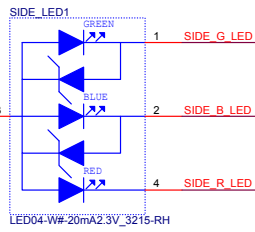


2016.08.02 Add +12V LED 0.1uF

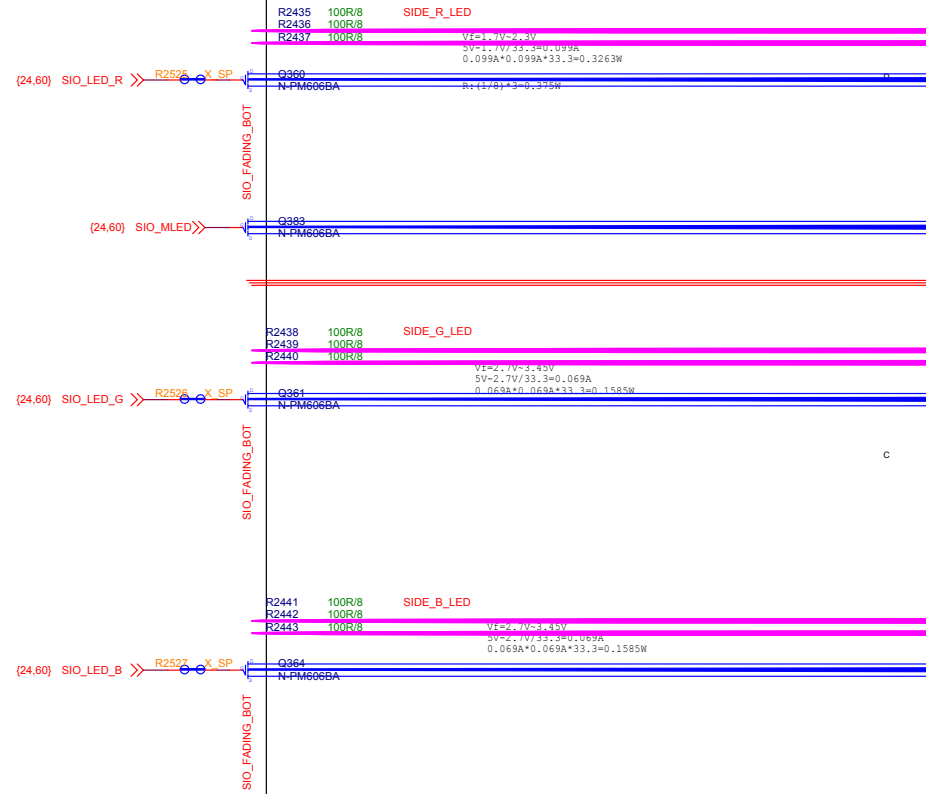


2016.08.02 stuff ESD

BOARD SIDE
LED *8



2018/11/26
R2525, R2526, R2527 are changed from 0ohm to copper by cost down



MICRO-STAR INT'L CO.,LTD.

Title RGB LED Control

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Date: Tuesday, December 18, 2018

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OPTION BOM PARTS

60 Level

A B C D E

PCIE X16 SLOT					
PCIE X8 SLOT				FOOTPRINT SLOT_PCIEXP100_5 可包容 SLOT_PCIEXP100_3	
REAL USB Type A				鍍金	
SOLID CAP 270u16				FOOTPRINT C_F3_5_D8_H12 因為機構無法使用 請注意! C_F3_5_D8_H9 可包容 C_F3_5_D8_H8	
SOLID CAP 560u6.3				FOOTPRINT C_F2_5_D6_3_H9_5 可包容 C_F2_5_D6_3_H9	
SOLID CAP 470u6.3				FOOTPRINT C_F2_5_D6_3_H9_5 可包容 C_F2_5_D6_3_H9	
SOLID CAP 100u16				FOOTPRINT C_F2_5_D6_3_H6 可包容 C_F2_5_D6_3_H5	
MEM SLOT				FOOTPRINT DDRIV_D288_1_T 可包容 DDRIV_D288	
MKTG Label					
PCH SINK					
MOSN +IO					
MOSW					
PS2_USB					
HDMI_USB					
LAN_USB					

5010 Level

A B C D E

FCH					
M.2 SLOT				FOOTPRINT SLOT_NGFFCARD67_31 可包容 SLOT_NGFFCARD67_2	
USB Type C MUX					
USB Gen2 Redriver					
0 Ohm (0402)					
LED					

5020 Level

A B C D E

LED

60 Level

A B C D E

Audio cover					
Audio Jack					
M.2 SCREW					
PCIE X4 SLOT					

		MICRO-STAR INT'L CO.,LTD.	
Title BOM Option			
Size	Document Number MS-7C02..		
Date: Tuesday, December 18, 2018			

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Rev 20

